55:132/22C:160 HPCA
Spring 2011
Fourth Homework Assignment
Due: Thursday, February 24, in class

This assignment is based upon the following code segment ,which represents the body of the inner-most loop of a matrix multiply program, similar to the one that you analyzed in the last assignment. It is assumed that the integer instructions for loop control and address generation are processed by a separate functional unit so this assignment will consider only the floating point operations, as shown:

```
L.D     F0, 0(R1)     // F0 ←B[k][j] (load)
L.D     F2, 0(R2)     // F2 ← A[i][k] (load
L.D     F4, 0(R3)     // F4 ← C[i][j] (load)
MUL.D   F0, F2, F0    // F0 ← A[i][k] * B[k][j]
ADD.D   F4, F0, F4    // F4 ← C[i][j] + F0
S.D     F4, 0(R3)     //  Store F4 to C[i][j]
```

1. Calculate the execution time for six iterations of this loop body on the diversified pipeline shown in figure A.31 (page A-50) of the text. Assume that all relevant forwarding paths are implemented.

2. Now consider the execution of the loop body on the processor shown in Figure 2.9 (Page 94) that utilizes Tomasulo's algorithm for dynamic scheduling. As in problem 1, assume that the FP Adder is pipelined with 4 stages and the FP multiplier is pipelined with seven stages. Assume that at most one instruction can be issued to a reservation station per cycle, and that FP load operations complete (to a FLB) in one cycle. Also, assume that FP stores can be overlapped with subsequent execution so once a result has been written to a SDB, the processor no longer needs to worry about it.
    a. Show the cycle by cycle operation of Tomasulo's algorithm for two iterations of the loop body.
    b. Based upon your answer to a, estimate the total execution time for six iterations of the loop