55:132/22C:160
Spring, 2011
Second Homework Assignment
Due: Wednesday, Feb. 9 by 11:59 p.m. (e-mail submission)

The objective of this assignment is to gain familiarity with Verilog modeling and the ModelSim Verilog tools.

You are to modify the Verilog example (Fibonnaci number generator), given in the Lecture Notes section of the course web page, as follows:

1) The *fibNumberGen* module should be modified so that the time required to compute fib(N) is proportional to N. Specifically the module should take 20 nsec. to compute fib(0) and 20(N) nsec. to compute fib(N) for N>0. The module should hold the *done* output high for 10 nsec. after the new value is stable on the *num* output. (This 10 nsec. is in addition to the time required to compute the result).

2) Modify the *numberGen* module to replace the *run* input with a *count* input. At simulation time 0, the *num* output of the module should be 0. Then for each posedge (0->1) transition on the *count* input, the module should increment the *num* output by one after a delay of 20 nsec. As with the original *numberGen* module, the *ready* output should be held high for 10 nsec. after each new count value is stable on the *num* output.

3) Now develop a modified version of the *fibTop* module that uses an instance of the modified *numberGen* module to test your modfied *fibNumberGen* module by computing and displaying all Fibbonnaci numbers from fib(0) until an overflow occurs. This module should operate as fast as possible, given the timing constraints of the modified *fibNumberGen* and *numberGen* modules.

Debug and test your modified design until it is working correctly. Then follow these submission instructions:

E-mail the Verilog source files *fibNumberGen.v*, *numberGen.v*, and *fibTop.v* containing your three modified modules, along with the *transcript* file that will be automatically generated by vsim when you run the simulation of fibTop, to**: hpca@engineering.uiowa.edu**