55:132/22C:160, Spring 2011
First Homework Assignment
Due: Thursday, January 27, in-class

In questions 1-3 below you are to make sense of Figure 1, which presents the performance of selected processors and a fictional one (Processor X), as reported by *www.tomshardware.com*. For each system, two benchmarks were run. One benchmark exercised the memory hierarchy, giving an indication of the speed of the memory for that system. The other benchmark, Dhrystone, is a CPU-intensive benchmark that does not exercise the memory system. Both benchmarks are displayed in order to distill the effects that different design decisions have on memory and CPU performance.

Chip	# of cores	Clock frequency (MHz)	Memory performance	Dhrystone performance
Athlon 64 X2 4800+	2	2,400	3,423	20,718
Pentium EE 840	2	2,200	3,228	18,893
Pentium D 820	2	3,000	3,000	15,220
Athlon 64 X2 3800+	2	3,200	2,941	17,129
Pentium 4	1	2,800	2,731	7,621
Athlon 64 3000+	1	1,800	2,953	7,628
Pentium 4 570	1	2,800	3,501	11,210
Processor X	1	3,000	7,000	5,000

Figure 1. Performance of several processors on two benchmarks.

1. Make the following calculations on the raw data in order to explore how different measures color the conclusions one can make.

   a. Create a table similar to that shown in Figure 1, except express the results as normalized to the fastest application for each benchmark.

   b. Calculate the geometric mean of the normalized performance of the dual processors and the geometric mean of the normalized performance of the single processors for the memory benchmark.

2. Imagine that your company is trying to decide between a single-processor system and a dual-processor system. Figure 1gives the performance on two sets of benchmarks—a memory benchmark and a processor benchmark. You know that your application will spend 30% of its time on memory-centric computations, and 70% of its time on processor-centric computations.

   a. Calculate the weighted performance of the benchmarks for the Pentium 4 and Athlon 64 X2 3800+.

   b. How much speedup do you anticipate getting if you move from using a Pentium 4 to an Athlon 64 X2 3800+ on a memory-intensive application suite?

3. Your company has just bought a new dual Pentium processor, and you have been tasked with optimizing your software for this processor. You will run two applications on

this dual Pentium, but the resource requirements are not equal. The first application needs 75% of the resources, and the other only 25% of the resources.

a. Given that 60% of the first application is parallelizable, how much speedup would you achieve with that application if run in isolation?

b. Given that 95% of the second application is parallelizable, how much speedup would this application observe if run in isolation?

c. Given that 60% of the first application is parallelizable, how much *overall system speedup* would you observe if you parallelized it, but not the second application?

d. How much overall system speedup would you achieve if you parallelized both applications, given the information in parts (a) and (b)?

4. Using the SPEC web site (www.spec.org) and/or any other resources of your choosing answer the following questions:

a. In what ways does the SPEC CPU2006 benchmark suite constitute a more contemporary and representative computational mix than its predecessor, SPEC2000? List as many as you can.

b. Are the reference times for SPEC CPU2006 performance ratios based on the same reference machine as SPEC 2000?

c. SPEC CPU2006 reports two different performance metrics: base and peak. What is the difference between these?

5. Assume the following instruction mix for a MIPS-like RISC instruction set: 15% stores, 25% loads, 15% branches, and 35% integer arithmetic, 5% integer shift, and 5% integer multiply. Given that loads and stores require two cycles, branches require four cycles, integer ALU instructions require one cycle, and integer multiplies require ten cycles, compute the overall CPI.

6. Given the parameters of the previous problem, consider a compile-time optimization that converts multiplies into a sequence of shift and add instructions. For this instruction mix, 50% of the multiplies can be converted to shift-add sequences with an average length of five instructions. Assuming no change in clock frequency, compute the change in instructions per program, cycles per instruction, and overall program speedup due to the compiler optimization.