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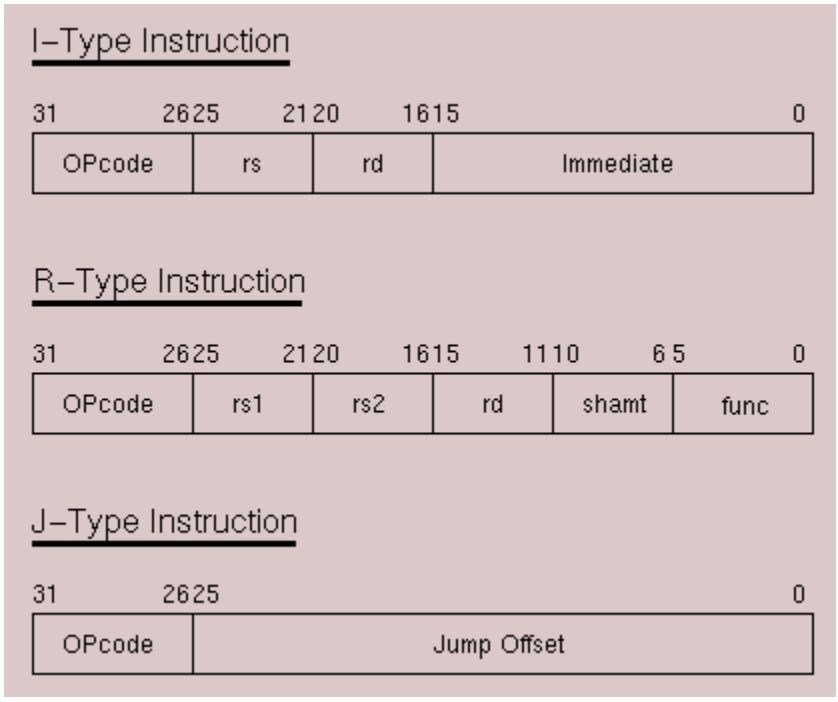
ISA for Discussion of 5-stage Pipeline

Machine Characteristics

```
word length:                    32 bit
general purpose registers:      32  ([R0] = 0)
address space:                  2^32 = 4 GByte
address resolution:             byte
operand lengths:                16 bit immediate / word
addressing modes:               immediate, displacement
instruction formats:
```



Instruction Set (DLX Subset)

Mnemonic	Type	Opcode	Func	Assembly	Semantics
lw	I	0x23		lw rd,imm(rs)	rd <- mem[[rs]+imm]
sw	I	0x2b		sw imm(rs),rd	mem[[rs]+imm] <- [rd]
add	R	0x0	0x20	add rd,rs1,rs2	rd <- [rs1] + [rs2]
addi	I	0x8		addi rd,rs,imm	rd <- rs + signext##imm
sub	R	0x0	0x22	sub rd,rs1,rs2	rd <- [rs1] [rs2]
mul	R	0x0	0x18	mul rd,rs1,rs2	rd <- [rs1] * [rs2]
and	R	0x0	0x24	and rd,rs1,rs2	rd <- [rs1] & [rs2]
or	R	0x0	0x25	or rd,rs1,rs2	rd <- [rs1] | [rs2]
sll	R	0x0	0x0	sll rd,rs1,shamt	rd <- [rs1] << shamt

srl	R	0x0	0x2	srl rd,rs1,shamt	rd <- [rs1]>> shamt
beqz	I	0x4		beqz rs,imm	pc <- [rs]="=0" ? [npc]+signext##imm : [npc]
bnez	I	0x5		bnez rs,imm	pc <- [rs]!="0" ? [npc]+signext##imm : [npc]
j	J	0x2		j offset	pc <- [npc]+signext##offset
nop	R	0x0	0x0	nop	do nothing
hlt	I	0xd		hlt	halt execution