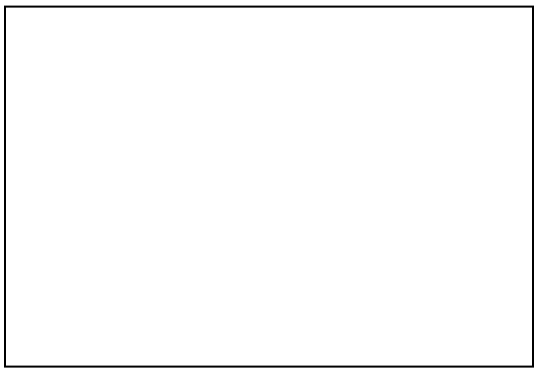


EZZBM01

802.15.4 Full Function Device (FFD) Module

Product Information Data Sheet

SEPTEMBER 2004

Device features

- IEEE 802.15.4 compliant (2450MHz specification)
- Compliant with worldwide regulations covered by EN 300 440 (Europe), FCC CFR47 Part 15 (US), and ARIB STD T-66 (Japan)
- UART interface to Host Controller
- OEM single-board module with integrated processor and 32KB Flash
- In-system programmable for firmware upgrade/application customization
- Configurable I/O of up to 16 ports
- RF operation: 16 channels at 2.4GHz
- Low data rate: up to 250kbps
- Operating voltage: 3.3VDC nominal input, option for 3V battery
- External antenna
- Operating temperature range: -20°C to 70°C
- Compact surface mountable module: approx. 24mm x 16mm

General Description

The EZZBM01 is a compact single-board module compliant to the 2450MHz specification of IEEE 802.15.4.

The EZZBM01 is a Full Function Device (FFD) designed to be used as a serial RF module to a Host system.

The EZZBM01 module uses CC2420 RF Transceiver and ATmega32L AVR RISC Processor.

Applications

- Remote switching
- Remote sensing / telemetry
- Keyless entry
- Wireless remote control
- Personal Area Networks
- Home/Building automation
- Industrial controls
- PC peripherals

Key Features

Radio

- Utilizes CC2420, Chipcon's single-chip 802.15.4 compliant and Zigbee-ready RF transceiver
- 16 DSSS channels at 2400 to 2483.5 MHz
- Output power from -25dBm to 0dBm
- -94dBm receiver sensitivity at PER<1%

Baseband

- 802.15.4 MAC hardware support
- 250 kbps effective data rate, 2Mchips/s chip rate
- 128 (RX) + 128 (TX) byte data buffering
- Hardware MAC encryption (AES-128)

This document contains information on a pre-production product. Specifications and information contained herein are subject to change without notice.

Processor/Firmware

- Delivered with Chipcon 802.15.4 MAC
- Firmware upgradeable via SPI (AVRISP)
- Options available by firmware upgrade: custom application MAC, AT command interface
- Host controller UART interface up to 1Mbps
- Up to 8 MIPS throughput at 8MHz
- User configurable I/O pins by firmware
- JTAG debugging using Atmel JTAGICE

Power

- Power source options selectable at production: 3.3VDC using internal voltage regulator or 3V battery with on-chip battery monitor

Block Diagram

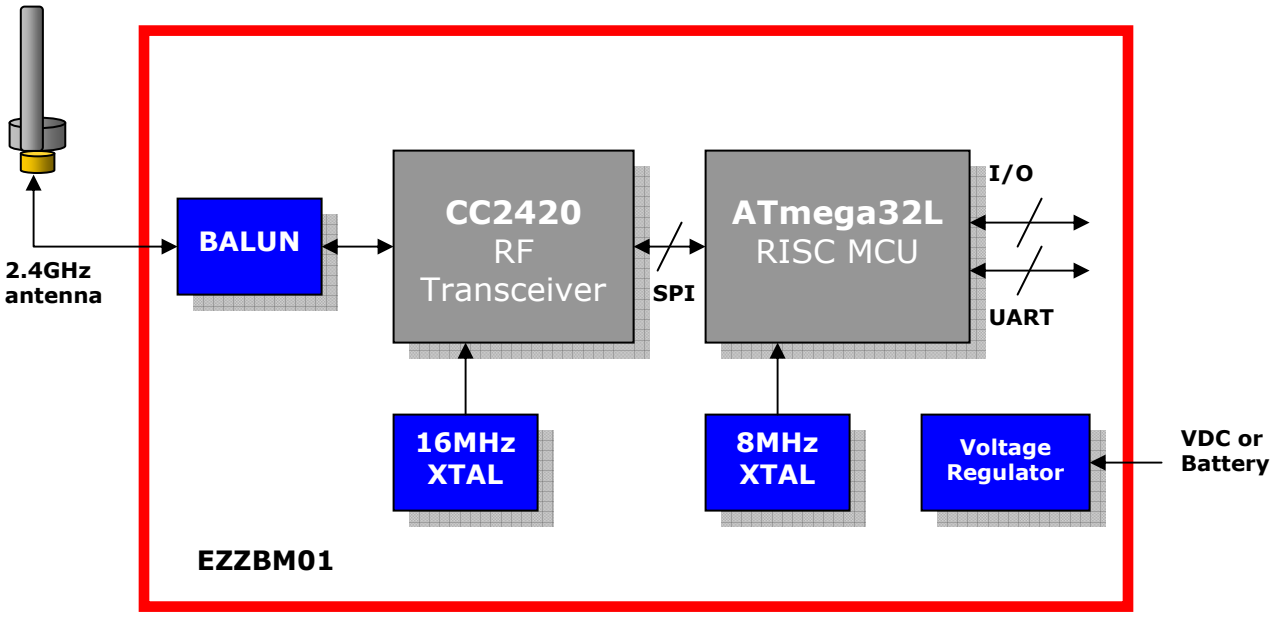
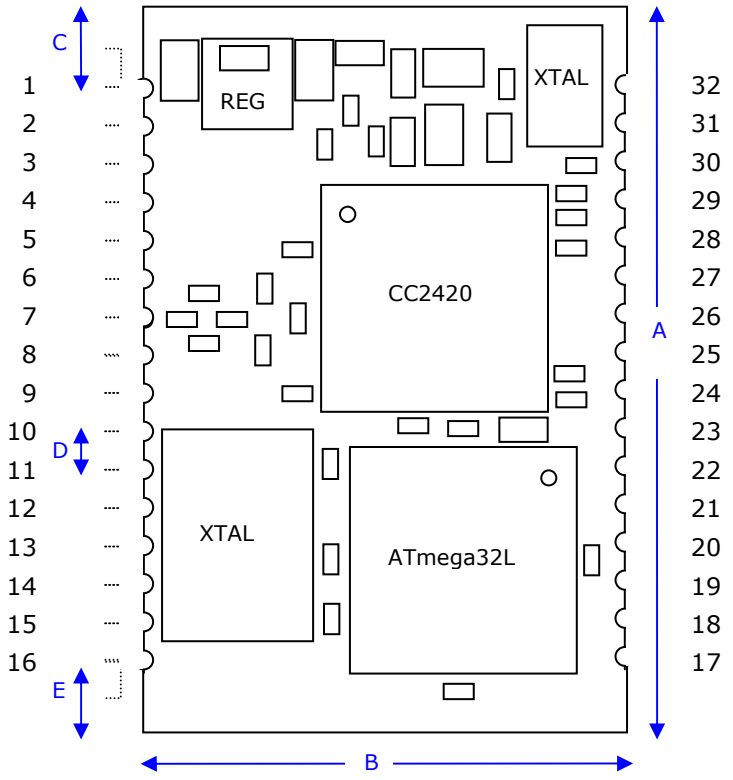


Figure 1: EZZBM01 Block Diagram

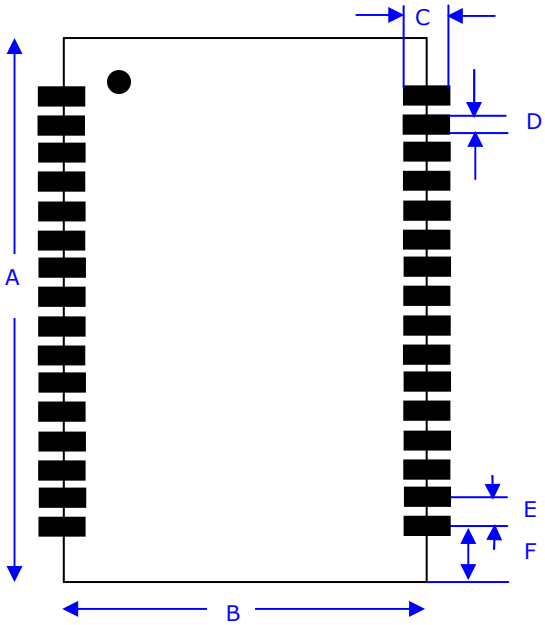
Component Layout and Device Pinout Diagram



	All dimensions in mm.		
	MIN	TYP	MAX
A		25	
B		16.5	
C		2.8	
D		1.27	
E		3.15	

Figure 2: EZZBM01 Dimensions and Pinout

Layout Recommendations



	All dimensions in mm.		
	MIN	TYP	MAX
A		25	
B		16.5	
C		2.0	
D		0.8	
E		1.27	
F		3.15	

Figure 3: EZZBM01 Pad Layout

Device Terminal Functions

Terminal	Terminal Name	I/O	Description
1	DVDD		DC 3.3V power or 3V battery
2	DVDD		
3	DGND		Digital Ground
4	NC		Not connected
5	NC		
6	AGND		Analog Ground (connected to DGND internally)
7	RF	I/O	Antenna RF port
8	AGND		
9	PB0/RXD	I/O	Port B GPIO or UART RXD [1]
10	PB1/TXD	I/O	Port B GPIO or UART TXD [1]
11	PB2/CTS	I/O	Port B GPIO or UART CTS; also configurable as interrupt INT [1]
12	PB3/RTS	I/O	Port B GPIO or UART RTS [1]
13	PC0/TCK	I/O	Port C GPIO or JTAG TCK [2]
14	PC1/TMS	I/O	Port C GPIO or JTAG TMS [2]
15	PC2/TDO	I/O	Port C GPIO or JTAG TDO [2]
16	PC3/TDI	I/O	Port C GPIO or JTAG TDI [2]
17	DGND		
18	PA/ADC7	I/O	Port A GPIO or ADC channel [3]
19	PA/ADC6	I/O	Port A GPIO or ADC channel [3]
20	PA/ADC5	I/O	Port A GPIO or ADC channel [3]
21	PA/ADC4	I/O	Port A GPIO or ADC channel [3]
22	PA/ADC3	I/O	Port A GPIO or ADC channel [3]
23	PA/ADC2	I/O	Port A GPIO or ADC channel [3]
24	PA/ADC1	I/O	Port A GPIO or ADC channel [3]
25	PA/ADC0	I/O	Port A GPIO or ADC channel [3]
26	DGND		
27	RESETN	I	Low asserted Reset input, with internal pullup resistor, may be left unconnected
28	SCLK	O	SPI clock [4]
29	DVDD_OUT		Voltage Regulator Output
30	MOSI	I	SPI Master Out Slave In [4]
31	MISO	O	SPI Master In Slave Out [4]
32	DGND		

Notes:
1: Port B is connected internally to PD of ATmega32L.
2: Port C is connected internally to PC of ATmega32L. May be used for ICE debugging.
3: Port A is connected internally to PA of ATmega32L
4: To be used only for in-system programming of the AVR Flash only. Not intended for connecting an external SPI device. Refer to AVRISP Manuals.

Table 1: Device Terminal Functions

Electrical Characteristics

Absolute Maximum Ratings [1]

Parameter	Symbol	Min	Max	Units
Power Supply Voltage	DVDD		12	V
Input Pin Voltage	VIN		VDDIO + 0.3 max 3.6	V
Input RF Level	VRF		10	dBm
Storage Temperature		-50	150	°C
Lead Temperature			260	°C

Table 2: Absolute Maximum Ratings

Note 1: The absolute maximum ratings should under no circumstances be violated. Stress exceeding one or more of the limiting values may cause permanent damage to the device.

Operating Conditions

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply Voltage	DVDD	DC input	3.1	3.3	10	V
		Battery input	2.7	3.0	3.6	V
Supply Current	I_{CC}	0 dBm, Active		30		mA
		-24 dBm, Active		20		mA
		Receive		32		mA
		Idle		6		mA
		Power down			30	µA
Operating Temperature	T_{OPR}		-20	27	70	°C

Table 3: Operating Conditions

Electrical Specifications

T_A = 27°C, DVDD = 3.3V (DVDD_OUT = 3.0V) unless otherwise noted

Parameter	Symbol	Condition	Min	Typ	Max	Units
Radio Characteristics						
RF Frequency Range	F		2400		2483.5	MHz
Transmit rate		Bit	250		250	kbps
		Chip	2000		2000	kchips/s
Nominal Output Power	Pout		-3	0		dBm
Receiver Sensitivity		PER = 1%	-90	-94		dBm
Channel Spacing		16 channels		5		MHz

Spurious Emissions		Transmit, 1-12.75GHz		-30		dBm
		Receive, 1-12.75GHz		-47		dBm
Frequency Tolerance			-300		300	KHz
Symbol Rate Tolerance					120	ppm
DC Characteristics						
Input Low Voltage	V_{IL}		-0.5		0.6	V
Input High Voltage	V_{IH}		1.8		3.5	V
Output Low Voltage	I_{OL}	I_{OL}=10mA			0.5	V
Output High Voltage	I_{OH}	I_{OH}=-10mA	2.2			V
IO Pin Pullup Resistor	R_{PU}		20		50	kΩ
ADC Input Resistance	R_{AIN}			100		MΩ
AC Characteristics						
UART Baud rate	BR		2400		1M	Bps
UART Error	U_{ERR}	9600 baud		0.2		%
		57.6 kbaud		-3.5		%
		115.2 kbaud		8.5		%
		0.5 Mbaud		0		%
ADC Conversion Time			13		260	µs
ADC input bandwidth				38.5		kHz

Table 4: Electrical Specifications

Applications

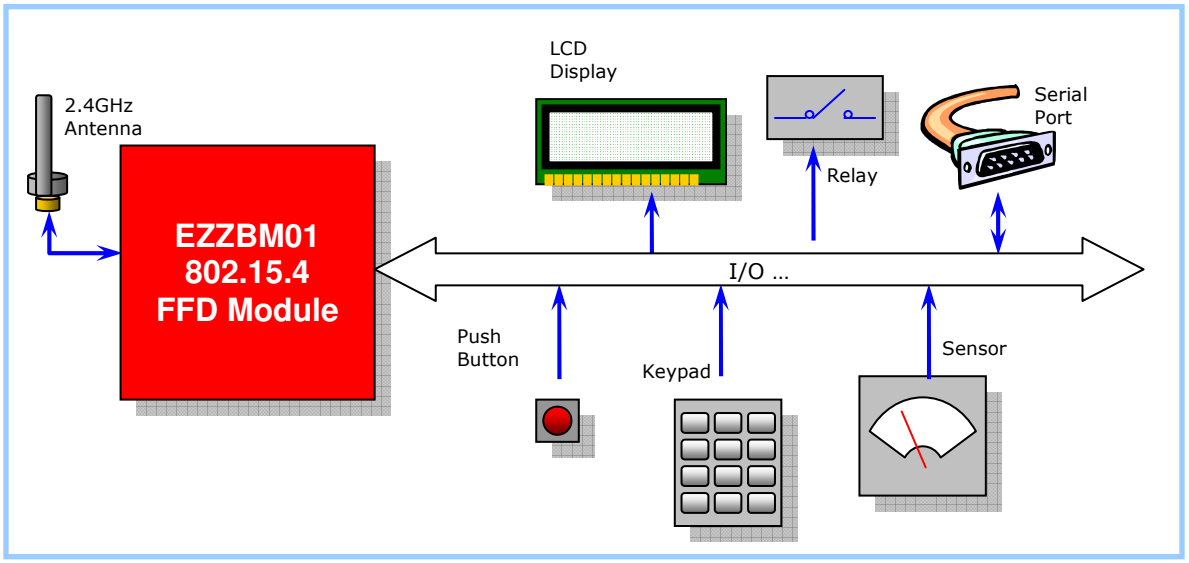


Figure 4: EZZBM01 General Application Diagram

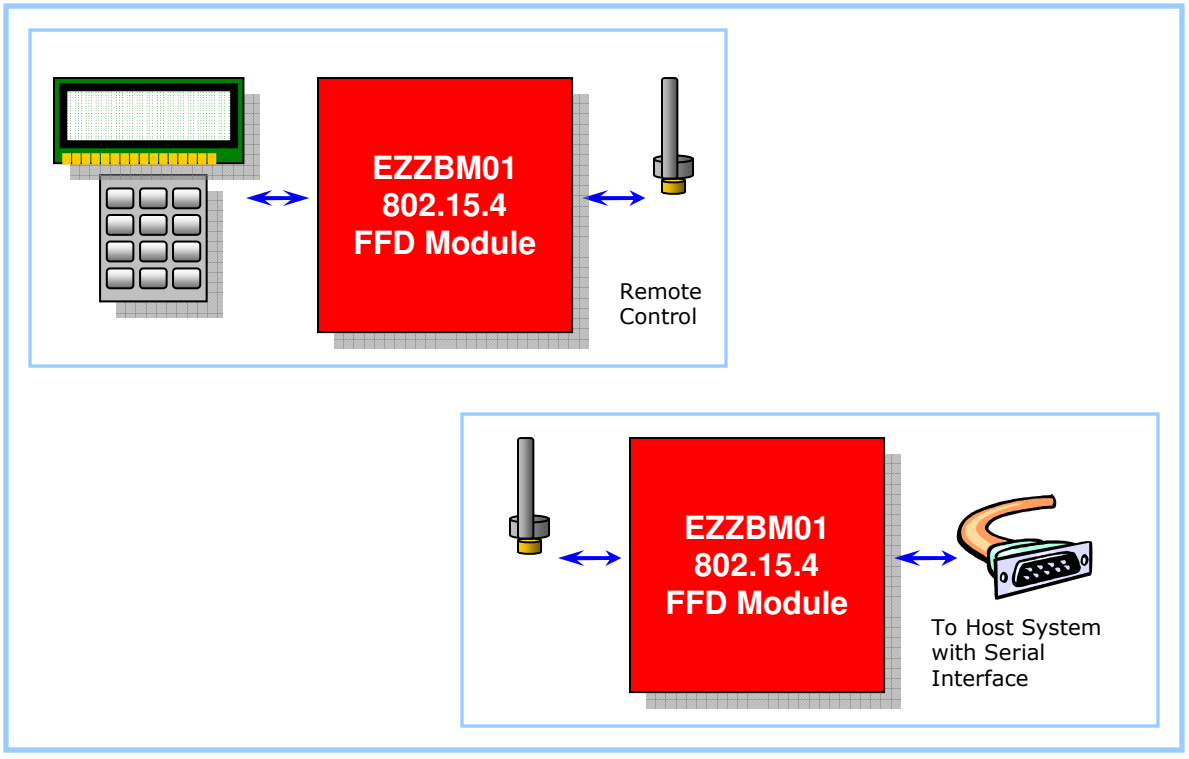


Figure 5: EZZBM01 Sample Application: Wireless Remote Control

Interface Description

General Purpose I/O

A maximum of 16 digital I/O are provided by EZZBM01 for general purpose interface to the application. Port A corresponds to PA of ATmega32L; Port B uses PD; and Port C uses PC. These I/O are configurable via Firmware.

The GPIO ports support alternate functions, namely UART, ADC and interrupt. The module is configured by default to 8-bit GPIO at Port A, 4-wire UART at Port B and 4-bit GPIO at Port C.

UART

UART is supported at bits 3~0 of Port B. ATmega32L provides the hardware circuitry for a 2-wire UART, which can be extended to a 4-wire UART by software control.

Baud rate support is up to 1Mbps for 8MHz internal clock.

This serial interface can be used by a Host Controller to send messages/commands for a multi-processor communication. The Host may send, for example, AT commands to transmit data wirelessly using the module.

See ATmega32L Data Sheet for further details about its UART interface.

Interrupt

An external interrupt signal is supported by the module at bit 2 of Port B. This may be used by application peripherals to request immediate processing from the ATmega32L.

For example, the module may go to a Power Down or Sleep state to lower its power consumption. A keypad press may produce an interrupt to “wake” the module.

ADC

An 8-channel 10-bit ADC is provided at Port A. These may be used as analog input from various analog sources, such as sensors. Internal reference voltage is provided on-chip by the processor.

See ATmega32L Data Sheet for further details about its ADC interface.

SPI

The SPI interface is provided for In-System programming of ATmega32L using AVRISP and control of CC2420. *The interface should not be used to connect to an external SPI device.*

JTAG

The IEEE 1149.1 JTAG interface provides on-chip debugging of ATmega32L using JTAGICE.

Antenna

The antenna port is a single-ended port. Internal BALUN and matching are provided on the module to convert the RF signal to a differential signal required by CC2420. A general purpose 2.4GHz antenna may be connected to the antenna port.

Note that AGND or Analog Ground is for RF grounding and not for ADC grounding.

Power

Two power options are available for the module – a general 3.3V and above DC input or a 3V battery supply input. EZZBM01 is the standard module using the general DC supply. EZZBM01-01 is the module for a 3V battery supply.

EZZBM01 uses an internal voltage regulator to convert up to 10V DC input to its 3V internal operating voltage.

This internal regulator is not populated in the EZZBM01-01 and, hence, an ordinary 3V battery may be used to supply power to the module. A battery voltage monitor is instead provided internally.

DVDD_OUT is connected to the output of the 3V regulator and may be used to supply power to external peripherals. The regulator is able to supply 250mA (including the module) with maximum dropout up to 0.8V. To ensure proper operation at high current applications, set DVDD greater than 4V.

Firmware Description

The default firmware shipped with the module is a FFD MAC that includes a custom/extended AT command set. This enables the Host application to communicate to the module similar to a common modem. Communication is performed serially thru the full-duplex UART.

AT Command Support

The AT commands provide a simple command set that serves as an interface of the upper layers to the MAC layer primitives. The Host controller handles processor communication, RF transceiver control, PAN association and data transfer using the command set.

The AT commands supported by EZZBM01 include basic commands, as well as proprietary command sets particular to the module. Refer to the following section for the command reference.

LR-WPAN Operation

EZZBM01 is able to participate in a WPAN as a PAN coordinator or device in a star or peer-to-peer topology through external Host control. However, no upper layer processing, other than those defined in the MAC and PHY layers, are handled by the default firmware. Instead, the firmware provides all necessary interface primitives[1] for the module to associate/communicate with other FFDs and RFDs (Reduced Function Device) within the PAN range.

All EZZBM01 devices are assigned unique IEEE addresses and are used to identify itself to the PAN. The addresses are assigned during production. Address recognition may be handled optionally in hardware by CC2420.

Data Transfer

Transfer of data are likewise handled using interface primitives. Data requests and indication are provided for Host data control.

General Hardware Control

Host and Module processors communicate directly using commands/responses sent through UART. The command/response set is given in the following section.

Control for the PHY layers are likewise handled using interface primitives. These may include settings for output power, channel frequency, CCA mode, etc, which are set by writing to the appropriate CC2420 registers. The status of the MAC/PHY layers may also be provided through interface primitives, which reads the appropriate CC2420 registers and returns the result to the Host.

Note, however, that even though the module supports the abovementioned low-level register access, the default firmware shipped with the module may not include such functionality. Instead, the default firmware is to provide high-level system functionality access for the module.

Firmware Customization

A Development Kit software, currently under development, will allow the application developer to select the feature support of EZZBM01. This permits the developer to fully customize EZZBM01 depending on the application, even configuring it as a RFD, performing low-level MAC/PHY access and/or embedding a custom application.

Application Notes are available to OEM developers on how to build custom applications on top of the MAC layer.

[1] The interface primitives are generally software API for interfacing the MAC/PHY primitives to the Host application. A command/message sent through UART directly translates to one or more layer primitives to carry out the desired functionality.

Command Reference

The AT command set of the default EZZBM01 firmware includes General/Macro commands that provide high-level PAN functionalities, Support commands to supplement the Macro commands and Control commands needed for module control.

All commands require an "AT" string prefix. Sequence of AT commands in one line is not supported. Parameters on command line are also not supported. Instead, required parameters need to be written to corresponding S-Registers.

General / Macro Commands

PAN Start
- P0 – Start a non-beacon PAN
  Required parameters:
  - Logical channel (S1)
  - Security enable (S2)
- P1 – Start a beacon enabled PAN
  Required parameters:
  - Logical channel (S1)
  - Security enable (S2)

PAN Associate
- D – Device to associate to PAN
  Required parameters:
  - Logical channel (S1)
  - Security enable (S2)
- A – Association response from Host
  Required parameters:
  - Device address (S3)
  - Associated address (S4)
  - Status of association (S5)
  - Security enable (S2)

PAN Disassociate
- H0 – Associated device to leave PAN
  Required parameters:
  - Transmit options (S2)
- H1 – Coordinator instructing device to leave PAN
  Required parameters:
  - Device address (S3)
  - Transmit options (S2)

Data Transmit
- T0 – Send to coordinator
  Required parameters:
  - Message length (S6)
  - Message payload (S7)
  - Transmit options (S2)
- T1 – Send to node
  Required parameters:
  - Destination short address (S3)
  - Message length (S6)
  - Message payload (S7)
  - Transmit options (S2)
- T2 – Send to peer (intra-PAN)
  Required parameters:
  - Destination short address (S3)
  - Message length (S6)
  - Message payload (S7)
  - Transmit options (S2)
- T3 – Send to peer (inter-PAN)
  Required parameters:
  - Destination short address (S3)
  - Destination PAN (S4)
  - Message length (S6)
  - Message payload (S7)
  - Transmit options (S2)
- T4 – Broadcast
  Required parameters:
  - Message length (S6)
  - Message payload (S7)
  - Transmit options (S2)

Reset
- Z – Reset

Support Commands

Register Access
- Sn? – Returns value of S-Register n
- Sn=value – Write value to S-Register n

Receiver Enable
- %ER – Module receiver enable

Data Poll Request
- %PR – Indirect data poll request for non-beacon PAN
  Required parameters:
  - Security enable (S2)

Channel Access
- %C0 – Active channel scan
- %C1 – Passive channel scan
- %C2 – Orphan scan
- %C3 – Orphan scan response
  Required parameters:
  - Orphan device address (S3)
  - Assigned short address (S4)
  - Security enable (S2)

ACL Access
- %A0 – Add to ACL (Access Control List) entry in EEPROM
  Required parameters:
  - ACL Entry descriptor (S7)
- %A1 – Remove from ACL entry
  Required parameters:

- Extended address (S3)

Control Commands

Identification
- I0 – Product Code string
- I3 – Firmware version string
- I4 – OEM-defined string

Power Management
- %MP0 – Module wake up
- %MP1 – Processor power down (sleep idle), wake up by RF/UART interrupt
- %MP2 – Transceiver power down, wake up by sending %MP0
- %MP3 – Module power down, wake up by reset only

UART Control
- &K0 – No flow control
- &K3 – RTS/CTS flow control
- #BDR=value – Sets baudrate to value*2400bps, valid values = 8, 12, 16, 24, 48, 96

Register Definitions

The following table defines the S-Registers required by the command set.

Name	Size	Description	Default
S1	1 byte	Logical channel: 11 to 26 for valid channels, 0xFF for first available channel	11
S2	1 byte	Bit 0: Security enable (1 – TRUE, 0 – FALSE) Bit 3~1: Security mode 0b000 – Unsecured 0b001 – ACL Mode 0b010 – Secured Mode 0b100 – Not in ACL List Bit 6~4: Security suite 0b000 – No security suite 0b001 – AES-CTR 0b010 – AES-CCM-128 0b011 – AES-CCM-64 0b100 – AES-CCM-32 0b101 – AES-CBC-MAC-128 0b110 – AES-CBC-MAC-64 0b111 – AES-CBC-MAC-32 Bit 7: S3 is 64-bit IEEE	0x00
S3	8 bytes	ADDRESS (16-bit short address or 64-bit extended IEEE address)	0xFFFFFFFFFFFFFFFF
S4	2 bytes	PAN ID or Short address	0xFFFF
S5	1 byte	Status / Capability information	-
S6	1 byte	Message payload length	0
S7	128 bytes	Payload	-

Table 1: S-Register Definition

Response Codes

The response codes are returned to the Host in response to commands from the Host and/or events from the transceiver requiring Host attention.

Response Code Format

The response code, sent serially via UART shall be two bytes long with the following format:

Service ID	Result/status code

Service ID

The service ID identifies the service primitive and/or command which the corresponding result/status code refers to.

ID	Service type
0xC0	Data Request
0xC1	Data Indication
0xC2	Data Confirm
0xC3	Reserved
0xC4	Associate Request
0xC5	Associate Indication
0xC6	Associate Response
0xC7	Associate Confirm
0xC8	Disassociate Request
0xC9	Disassociate Indication
0xCA	Disassociate Confirm
0xCB	Beacon Notify Indication
0xCC	Get Request
0xCD	Reserved
0xCE	Reserved
0xCF	Reserved
0xD0	Orphan Indication
0xD1	Orphan Response
0xD2	Reset Request
0xD3	Receiver Enable Request
0xD4	Receiver Enable Confirm
0xD5	Scan Request
0xD6	Communication Status Indication
0xD7	Set Request
0xD8	Start PAN Request
0xD9	Synchronization Request
0xDA	Synchronization Loss Indication
0xDB	Poll Request
0xDC	Poll Confirm
0xFF	Control Command

Result/Status Codes

The result codes give the status of the command or service primitive.

Code	Description
0x00	Success
0x04	Error
0x10	Baud rate is 19.2kbps
0x40	Baud rate is 28.8kbps
0x11	Baud rate is 38.4kbps
0x12	Baud rate is 57.6kbps
0x13	Baud rate is 115.2kbps
0x14	Baud rate is 230.4kbps
0xE0	Beacon was lost following a synchronization request
0xE1	The CSMA/CA has failed
0xE3	The attempt to disable the transceiver has failed
0xE4	The received frame induces a failed security suite according to the security suite
0xE5	The frame resulting from secure processing has an invalid length
0xE8	A parameter in the primitive is out of valid range
0xE9	No acknowledgement was received
0xEA	A scan failed to find network beacon
0xEB	No response data was available following a request
0xEC	Operation failed because short address was not allocated
0xED	A receiver enable request failed because it can not be completed within CAP
0xEE	A PAN identifier conflict has been detected
0xEF	A coordinator realignment command has been received
0xF0	A transaction has expired and its information discarded
0xF1	No capacity to store transaction
0xF2	Transmitter is enabled when attempting to enable receiver
0xF3	The appropriate key is not available in the ACL
0xF4	A SET/GET command is issued with an unsupported attribute

Ordering and Contact Information

Order Number	Description
EZZBM01	Standard Module, 3.3VDC input. MOQ is 1K. Leadtime: 8-10 weeks
EZZBM01-01	Module for 3V battery supply. MOQ is 1K. Leadtime: 8-10 weeks

References

IEEE std. 802.15.4™ - 2003: Wirelesss Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (LR-WPANs). IEEE Computer Society. Sponsored by the LAN/MAN Standards Committee.

http://www.ieee802.org/15/pub/TG4.html

SmartRF® CC2420 Preliminary Datasheet (rev1.1). 2004-03-22. Chipcon AS, Oslo NORWAY.

http://www.chipcon.com/files/CC2420_Data_Sheet_1_1.pdf

CC2420 802.15.4 MAC/PHY Software Layers (rev0.62). Chipcon AS, Oslo NORWAY.

http://www.chipcon.com/index.cfm?kat_id=6&dok_id=152

ATmega32L Datasheet: 8-bit AVR with 32K Bytes In-System Programmable Flash. 2003-12. Atmel Corporation, CA 95131 USA

http://www.atmel.com/dyn/products/product_card.asp?part_id=2015

AVR ISP In-System Programmer. Atmel Corporation.

http://www.atmel.com/dyn/products/tools_card.asp?tool_id=2726

JTAGICE Real Time In-Circuit Emulator. Atmel Corporation.

http://www.atmel.com/dyn/products/tools_card.asp?tool_id=2737

EAZIX, Inc.
Unit 301 Plaz@ Building B
6530 Northgate Avenue, Filinvest Corporate City
Alabang, Muntinlupa City
Philippines 1770
Tel: + 632 772-4941
+ 632 772-4942
+ 632 772-4943
Fax: + 632 772-4944
Website: http://www.eazix.com/
E-mail: info@eazix.com

