55:131 Introduction to VLSI Design
Project #4 -- Fall 2009

Code Coverage for Simple PCI Target with EDAC with Bursting
Due Date: Friday December 11, 2009

Introduction

This project will use code coverage metrics to aid in test bench development. You will need to compile and load your design with code coverage enabled. See the Questasim User's Guide and the "do" file on the website to learn how to enable code coverage.

Your goal is to run the simulation and analyze the results for statement, focused condition, and focused expression coverage for all design units. For the statements, focused conditions, or focused expressions that are not covered, you need to determine if a) the uncovered Verilog RTL is extraneous, b) the test bench is inadequate (i.e. it doesn't exercise the PCI target as well as it should), or c) the code is not reachable (i.e. necessary code but not reachable no matter what changes are made to the test bench. For example, the "default" case in a case statement). A full explanation of the function of the uncovered code is needed (for example, "a test is needed in which a read memory transaction is attempted with the address outside the valid range of the target", not "the statement on line 157 was not hit"). If it is possible to reach the uncovered code by modifying the RTL or the test bench, it is acceptable (but not necessary) to make the modification(s) and try the change. The website code is the Verilog from project 3.

Questions

1. Explain all compilation warnings from Questasim.
2. Explain in a few sentences what is meant by "conditions" and "expressions".
3. Has your investigation of the coverage results uncovered any requirements that the design doesn't adequately meet? If so, which requirements?
4. Does it make sense to measure code coverage on the test bench itself? Why or why not?

What to turn in:

The design should compile and run under Questasim. Submit the RTL design files annotated with your explanation for all uncovered statement, focused conditions, and focused expressions, the source code and test bench (if you have modified them), and the answers to the questions above. All files should be ascii text files that are zipped-up into one zip file. Submit the file to the ICON dropbox. Grading for this project will be as shown below.

Item	Goal	Description	Percentage
1	Enable Coverage		
1a	Compile, Optimize	vlog, vopt command successful	10
1b	Simulate	vsim –coverage successful	10
2	Coverage explanations		
2a	Statements	Statements explanations	20
2b	Conditions	Focused Conditions explanations	24
2c	FEC	Focused Expression explanations	8
3	Questions	1	3
		2	10
		3	10
		4	5
Total			100