55:131 Introduction to VLSI Design
Project #4 -- Fall 2010

Code Coverage of Up/Down Counter
Due Date: Friday December 10, 2010

Introduction

In this project we will create a test bench for an up/down counter and measure its thoroughness using code coverage. The up/down counter has the following features:

- 8-bit datapath
- resettable
- loadable
- count enable
- up/down control
- overflow and underflow outputs

Goals

- To write a test bench which tests the up/down counter's functionality.
- To measure the test bench's coverage of the up/down counter
- To interpret the coverage report and improve your test bench as needed
- To understand the up/down counter's functions.

Discussion:

Your test bench should ensure that the up/down counter works correctly. In addition, the thoroughness of your test bench shall be measured using "code coverage". Code coverage measures how well various constructs of the RTL are exercised by the test bench. Note that coverage does *not* indicate if the up/down counter works correctly, just that it was exercised.

The up/down counter RTL is provided on the website along with a "do" file. The "do" file on the website instruments the RTL and creates a coverage report. It is recommended that you re-use parts of the PCI target test bench as a starting point for your test bench (e.g. clock and reset generation).

Grading

Item	Description	Points	Comments
Coverage 1	Statement coverage	25%	The coverage will be multiplied by 25% for this part of the grade (i.e. if you achieve 100% coverage, you get all 25%)
Coverage 2	Focused Condition coverage	40%	The coverage will be multiplied by 40% for this part of the grade (i.e. if you achieve 100% coverage, you get all 40%)
Question 1	For each of the following inputs, state whether or not it must be synchronous with the clock: reset_b, load, enable, direction, and data.	5%	
Question 2	Sketch a "behavioral" schematic of the circuit	10%	Use an "8-bit flop", single flops, incrementer, decrementer, muxes, comparators, and logic gates as needed
Question 3	In the RTL generating the result, is the precedence among the reset, load, ena, and dir signals reasonable? Explain why or why not.	10%	If the precedence order could be improved, list the improvement and explain why it is better. If it cannot be improved explain why changing the order would make the design worse.
Question 4	Explain the difference between statement coverage, condition coverage, and toggle coverage	10%	Use the Modelsim User's Guide and Reference Manual for help

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What to turn in:

Submit your test bench code, coverage report, "do" file, and answers to the questions above to the ICON dropbox. The test bench (and RTL design, though it should not have changed) should compile and run under Modelsim/Questsim. All files should be ascii text files.