55:131 Introduction to VLSI Design
Project #1 -- Fall 2010
Master-Slave Flip-flop and Counter Built in SPICE
Due Date: Friday September 17, 2010

Introduction

In this project we will create a transistor-level model of a master-slave flip-flop, in SPICE. The flip-flop's setup, hold, and propagation delays will all be measured. All models and measurements will be done in SPICE.

Goals:

- Create a transistor-level model of a master-slave flip-flop
- Test the flip-flop's operation
- Measure its setup time
- Measure its hold time
- Measure its propagation delay
- Build a 2-bit synchronous counter
- Measure the counter's maximum operating frequency
- All work is done in SPICE

Description:

The first circuit is a master-slave flip-flop as shown in figure 1 and figure 1.32(e) in the textbook.

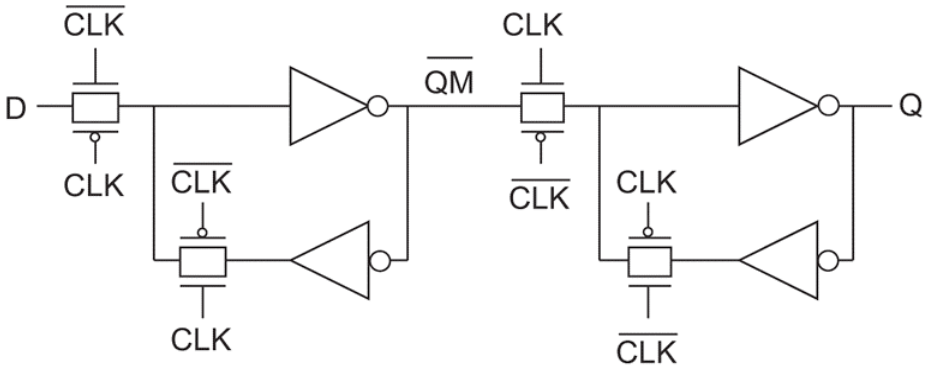

Figure 1: Master-Slave Flip-Flop

Using MicroSim SPICE, create the circuit as shown, using NMOS and PMOS transistors. The same transistor types should be used for the transmission gates and inverters. The transistor parameters should be as shown in the figures below. Use analog stimulus generators. Create the complemented clock signal(s) using inverters made from these same transistor types.

Measurements of the flip-flop's setup, hold, and propagation delays are done using SPICE. "Setup" is the minimum amount of time in which the input signal (D) must be stable before the rising edge of the clock and still have the flop operate correctly (i.e. the correct value on D is propagated to the output, Q). "Hold" is the minimum amount of time after the rising edge of the clock in which the input signal must be held in one state for that state to be propagated reliably to the output. "Propagation" is the delay from the rising edge of the clock input to the change in output.

The second circuit is a synchronous counter. The counter is constructed by cascading 2-flip-flops together, along with appropriate 2-input NAND gates to make the counter work properly.

Figure 2: NMOS parameters

Figure 3: PMOS parameters

Simulator:

Spectrum Software's Micro-Cap Evaluation version will be used for SPICE circuit simulations.

Discussion:

Flip-flops and latches are primitive design elements in VLSI devices. They are inferred from behavioral code, as we'll see in future projects. Timing for primitive elements like NAND gates and flip-flops is given in device libraries. The library information comes from SPICE simulations and measurements on real silicon. We'll measure timing using SPICE in this project.

Synchronous designs are very common in VLSI devices. The flip-flops (or latches) in synchronous circuits are all driven by the same clock signal, and the clear or preset pin to each flop is driven by a common signal. Almost any circuit can be made synchronous! Logic is generally easier to design, build, and debug when it is synchronous. EDA tools are also well suited to build and analyze synchronous logic.

Questions:

1) What are the setup, hold, and propagation delays for the flip-flop?
2) What is the maximum operating frequency of the counter?
3) Are the transistor parameter values chosen reasonable? Why or why not?
4) Are there any problems with this flip-flop?
5) What is the area of the D flip-flop (using lambda rules)?

What to turn in:

Turn in your circuit files and the answers to the questions above. All designs should run in Micro-Cap SPICE. If you have any special instructions for your simulation, turn them in too. All files should be .cir or ascii text files that are placed in the ICON dropbox for this project.

There is a 10% penalty for submissions that are up to 1 week late and 50% for submissions that are up to 2 weeks late. No submissions are allowed after 2 weeks beyond the project due date.