55:131 Introduction to VLSI Design
Project #1 -- Fall 2009
Flip-flop built from NAND gates, timing
Grading Key

Item	**Points**	**Comments**
Create a transistor-level model of a 2-input NAND gate (with parasitic elements)	5	Correct components
Test the transistor model of the NAND gate	10	NAND function
Measure its propagation delay	5	50% Vdd point, rise and fall
Design and create a master-slave flip-flop with clock enable from 2-input MUXes and NAND gates	10	Correct components
Test the flip-flop with clock enable	20	Flop function, output only changes on rising edge of clock both transitions on output tested
Questions 1) Are the parasitic values chosen reasonable (locations and values)? Why or why not? 2) Compare the transistor count of the D flip-flop with clock enable to figure 7.19b (with the MUX of figure 7.26) from the textbook. Name at least one advantage each flip-flop has over the other. 3) What are the setup, hold, and clock-to-output times for the D flip-flop with clock enable? Are there any problems with this flip-flop? 4) What is the area of the D flip-flop with enable (using lambda rules)?	 10 10 20 10	