Lecture 21: Packaging, Power, & Clock
Outline

- Packaging
- Power Distribution
- Clock Distribution
Packages

- Package functions
  - Electrical connection of signals and power from chip to board
  - Little delay or distortion
  - Mechanical connection of chip to board
  - Removes heat produced on chip
  - Protects chip from mechanical damage
  - Compatible with thermal expansion
  - Inexpensive to manufacture and test
Package Types

- Through-hole vs. surface mount

Diagram showing various package types including:
- 84-pin PLCC
- 14-pin DIP
- 44-pin PLCC
- 387-pin PGA Multichip Module
- 84-pin PGA
- 280-pin QFP
- 86-pin TSOP
- 40-pin DIP
- 560-pin BGA
- 296-pin PGA
Traditionally, chip is surrounded by *pad frame*
- Metal pads on 100 – 200 μm pitch
- Gold *bond wires* attach pads to package
- *Lead frame* distributes signals in package
- Metal *heat spreader* helps with cooling
Advanced Packages

- Bond wires contribute parasitic inductance
- Fancy packages have many signal, power layers
  - Like tiny printed circuit boards
- *Flip-chip* places connections across surface of die rather than around periphery
  - Top level metal pads covered with solder balls
  - Chip flips upside down
  - Carefully aligned to package (done blind!)
  - Heated to melt balls
  - Also called *C4* (Controlled Collapse Chip Connection)
Use many $V_{DD}$, GND in parallel
- Inductance, $I_{DD}$
Heat Dissipation

- 60 W light bulb has surface area of 120 cm$^2$
- Itanium 2 die dissipates 130 W over 4 cm$^2$
  - Chips have enormous power densities
  - Cooling is a serious challenge
- Package spreads heat to larger surface area
  - Heat sinks may increase surface area further
  - Fans increase airflow rate over surface area
  - Liquid cooling used in extreme cases ($$$$)
Thermal Resistance

- $\Delta T = \theta_{ja} P$
  - $\Delta T$: temperature rise on chip
  - $\theta_{ja}$: thermal resistance of chip junction to ambient
  - $P$: power dissipation on chip

- Thermal resistances combine like resistors
  - Series and parallel

- $\theta_{ja} = \theta_{jp} + \theta_{pa}$
  - Series combination
Example

- Your chip has a heat sink with a thermal resistance to the package of 4.0° C/W.
- The resistance from chip to package is 1° C/W.
- The system box ambient temperature may reach 55° C.
- The chip temperature must not exceed 100° C.
- What is the maximum chip power dissipation?

\[
\frac{(100 - 55) \text{ C}}{(4 + 1) \text{ C/W}} = 9 \text{ W}
\]
Temperature Sensor

- Monitor die temperature and throttle performance if it gets too hot
- Use a pair of pnp bipolar transistors
  - Vertical pnp available in CMOS

\[ I_c = I_s e^{\frac{qV_{BE}}{kT}} \rightarrow V_{BE} = \frac{kT}{q} \ln \frac{I_c}{I_s} \]

\[ \Delta V_{BE} = V_{BE1} - V_{BE2} = \frac{kT}{q} \left( \ln \frac{I_{c1}}{I_s} - \ln \frac{I_{c2}}{I_s} \right) = \frac{kT}{q} \left( \ln \frac{I_{c1}}{I_{c2}} \right) = \frac{kT}{q} \ln m \]

- Voltage difference is proportional to absolute temp
  - Measure with on-chip A/D converter
Power Distribution

- Power Distribution Network functions
  - Carry current from pads to transistors on chip
  - Maintain stable voltage with low noise
  - Provide average and peak power demands
  - Provide current return paths for signals
  - Avoid electromigration & self-heating wearout
  - Consume little chip area and wire
  - Easy to lay out
Power Requirements

- $V_{DD} = V_{DDnominal} - V_{droop}$
- Want $V_{droop} < +/- 10\%$ of $V_{DD}$
- Sources of $V_{droop}$
  - IR drops
  - $L \frac{di}{dt}$ noise
- $I_{DD}$ changes on many time scales
IR Drop

- A chip draws 24 W from a 1.2 V supply. The power supply impedance is 5 mΩ. What is the IR drop?
L di/dt Noise

- A 1.2 V chip switches from an idle mode consuming 5W to a full-power mode consuming 53 W. The transition takes 10 clock cycles at 1 GHz. The supply inductance is 0.1 nH. What is the L di/dt droop?

\[ \Delta I = \frac{(53 \text{ W} - 5 \text{ W})}{1.2 \text{ V}} = 40 \text{ A} \]

\[ \Delta t = 10 \text{ cycles} \times (1 \text{ ns} / \text{ cycle}) = 10 \text{ ns} \]

\[ L \frac{di}{dt} \text{ droop} = (0.1 \text{ nH}) \times \left( \frac{40 \text{ A}}{10 \text{ ns}} \right) = 0.4 \text{ V} \]
Bypass Capacitors

- Need low supply impedance at all frequencies
- Ideal capacitors have impedance decreasing with $\omega$
- Real capacitors have parasitic R and L
  - Leads to resonant frequency of capacitor

![Impedance vs Frequency Graph]

- 0.03 $\Omega$
- 1 $\mu$F
- 0.25 nH
Power System Model

- Power comes from regulator on system board
  - Board and package add parasitic R and L
  - Bypass capacitors help stabilize supply voltage
  - But capacitors also have parasitic R and L
- Simulate system for time and frequency responses
Frequency Response

- Multiple capacitors in parallel
  - Large capacitor near regulator has low impedance at low frequencies
  - But also has a low self-resonant frequency
  - Small capacitors near chip and on chip have low impedance at high frequencies
- Choose caps to get low impedance at all frequencies
Example: Pentium 4

- Power supply impedance for Pentium 4
  - Spike near 100 MHz caused by package L
- Step response to sudden supply current chain
  - 1st droop: on-chip bypass caps
  - 2nd droop: package capacitance
  - 3rd droop: board capacitance
Charge Pumps

- Sometimes a different supply voltage is needed but little current is required
  - 20 V for Flash memory programming
  - Negative body bias for leakage control during sleep
- Generate the voltage on-chip with a charge pump

\[
V_{\text{out}} = N \left[ \frac{C V_{\text{DD}} - \frac{I_{\text{out}}}{f}}{C + C_s} - V_t \right]
\]
Energy Scavenging

- Ultra-low power systems can scavenge their energy from the environment rather than needing batteries
  - Solar calculator (solar cells)
  - RFID tags (antenna)
  - Tire pressure monitors powered by vibrational energy of tires (piezoelectric generator)
- Thin film microbatteries deposited on the chip can store energy for times of peak demand
Clock Distribution

- On a small chip, the clock distribution network is just a wire
  - And possibly an inverter for clkb
- On practical chips, the RC delay of the wire resistance and gate load is very long
  - Variations in this delay cause clock to get to different elements at different times
  - This is called clock skew
- Most chips use repeaters to buffer the clock and equalize the delay
  - Reduces but doesn’t eliminate skew
Example

- Skew comes from differences in gate and wire delay
  - With right buffer sizing, clk\textsubscript{1} and clk\textsubscript{2} could ideally arrive at the same time.
  - But power supply noise changes buffer delays
  - clk\textsubscript{2} and clk\textsubscript{3} will always see RC skew

\begin{center}
\begin{tikzpicture}
\node (gclk) at (0,0) {gclk};
\node (clk1) at (-2,0) {clk\textsubscript{1}};
\node (clk2) at (2,0) {clk\textsubscript{2}};
\node (clk3) at (4,0) {clk\textsubscript{3}};
\draw (gclk) -- (clk1) -- (clk2) -- (clk3);
\draw (0.5 mm) to (clk1);
\draw (0.4 pF) to (clk1);
\draw (3 mm) to (gclk);
\draw (1.3 pF) to (gclk);
\draw (3.1 mm) to (clk2);
\draw (0.5 mm) to (clk2);
\draw (0.4 pF) to (clk2);
\draw (0.4 pF) to (clk3);
\end{tikzpicture}
\end{center}
Review: Skew Impact

- Ideally full cycle is available for work
- Skew adds sequencing overhead
- Increases hold time too

\[ t_{pd} \leq T_c - \left( t_{pcq} + t_{\text{setup}} + t_{\text{skew}} \right) \]

sequencing overhead

\[ t_{cd} \geq t_{\text{hold}} - t_{ccq} + t_{\text{skew}} \]
Solutions

- Reduce clock skew
  - Careful clock distribution network design
  - Plenty of metal wiring resources
- Analyze clock skew
  - Only budget actual, not worst case skews
  - Local vs. global skew budgets
- Tolerate clock skew
  - Choose circuit structures insensitive to skew
Clock Dist. Networks

- Ad hoc
- Grids
- H-tree
- Hybrid
Clock Grids

- Use grid on two or more levels to carry clock
- Make wires wide to reduce RC delay
- Ensures low skew between nearby points
- But possibly large skew across die
Alpha Clock Grids

Alpha 21064

Alpha 21164

Alpha 21264

gclk grid

Alpha 21064

Alpha 21164

Alpha 21264

gclk grid

21: Package, Power, and Clock  
CMOS VLSI Design 4th Ed.
H-Trees

- Fractal structure
  - Gets clock arbitrarily close to any point
  - Matched delay along all paths
- Delay variations cause skew
- A and B might see big skew
Itanium 2 H-Tree

- Four levels of buffering:
  - Primary driver
  - Repeater
  - Second-level clock buffer
  - Gater
- Route around obstructions
Hybrid Networks

- Use H-tree to distribute clock to many points
- Tie these points together with a grid

- Ex: IBM Power4, PowerPC
  - H-tree drives 16-64 sector buffers
  - Buffers drive total of 1024 points
  - All points shorted together with grid