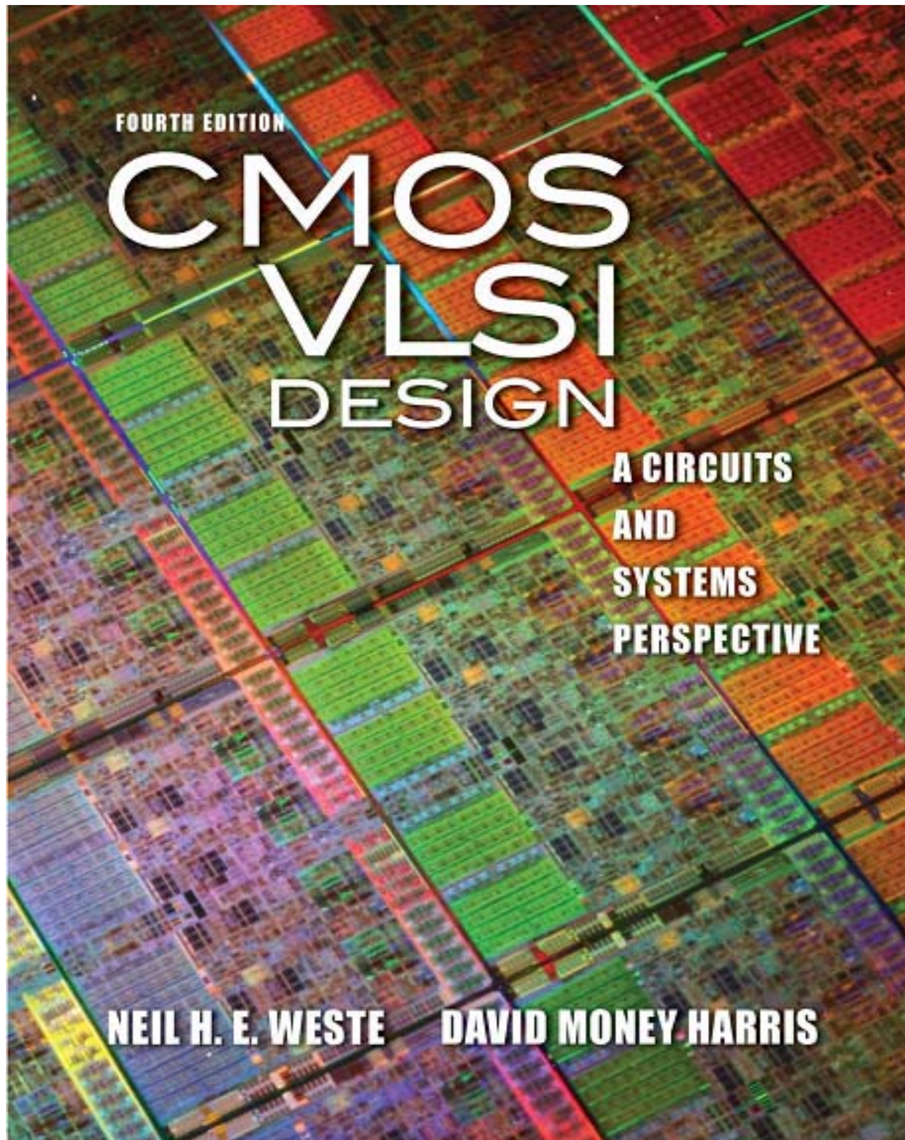


Lecture 0: Introduction

Introduction

- Integrated circuits: many transistors on one chip.
- *Very Large Scale Integration* (VLSI): bucketloads!
- *Complementary Metal Oxide Semiconductor*
  - Fast, cheap, low power transistors
- How to build a CMOS chip
  - CMOS transistors
  - Building logic gates from transistors
  - Transistor layout and fabrication

Introduction (cont'd)

- Course Outline
  - Physical, circuit, and logical design
  - Microarchitecture
  - Design issues
  - Verification
  - Test
  - Reliability

Introduction (cont'd)

- Course Overview
  - Design of digital integrated circuits (vs analog)
  - VLSI - Very Large Scale Integration
    - Millions of transistors
    - Many designers and verifiers for a large chip
  - CMOS – Complementary Metal Oxide Semiconductor
    - Both nmos and pmos transistors
    - Fast, cheap, low power transistors
    - Easily constructed in very large numbers

Introduction (cont'd)

- Course Overview (cont'd)
  - Practitioner's perspective
    - Real-world issues
  - Topic coverage will emphasize breadth over depth
    - Many types of tasks and jobs in VLSI
    - Common among all of them is attention to detail
  - Topic coverage, in general, will be bottom up
    - Physical -> structural -> behavioral

Administrative

- Instructor
  - Dave Matthews (not *that* Dave Matthews!)
  - Design engineer for Rockwell Collins (25 years)
  - PhD Student at U of I
  - Office 1126 SC, hours M,W,F 3:30 – 4:30
  - Email: david-matthews@uiowa.edu
- TA
  - Email: @uiowa.edu

Administrative (cont'd)

- Grading
  - Approximately 1 homework per week
  - 4 projects, all individual
  - 2 closed-book exams (1 mid-term, final)
  - Weighting
    - Homework 10%
    - Projects 10%, 15%, 15%, 10% respectively
    - Midterm 15%
    - Final 25%

Administrative (cont'd)

- Course webpage
  - Place to find syllabus, lecture notes, homework, etc
  - http://www.ece.engineering.uiowa.edu/grad/gradpages.htm
- Projects – Mentor Graphics tools
  - 4 projects, will be posted on website

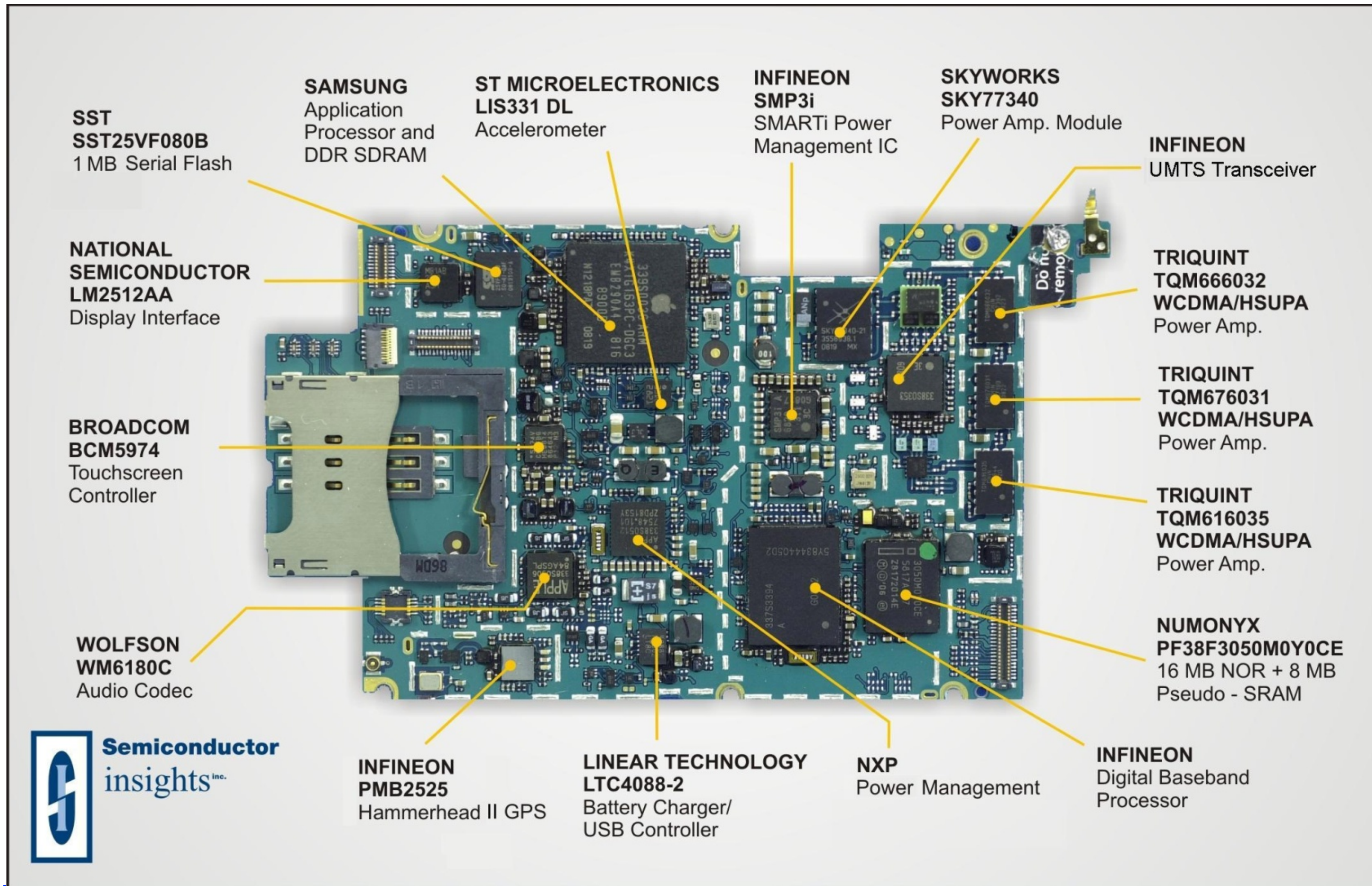
Administrative (cont'd)

- Collaboration
  - Discussion of the material is encouraged, but…
  - All students are expected to do their own work
- Disabilities
  - Please contact me (office hours or email)

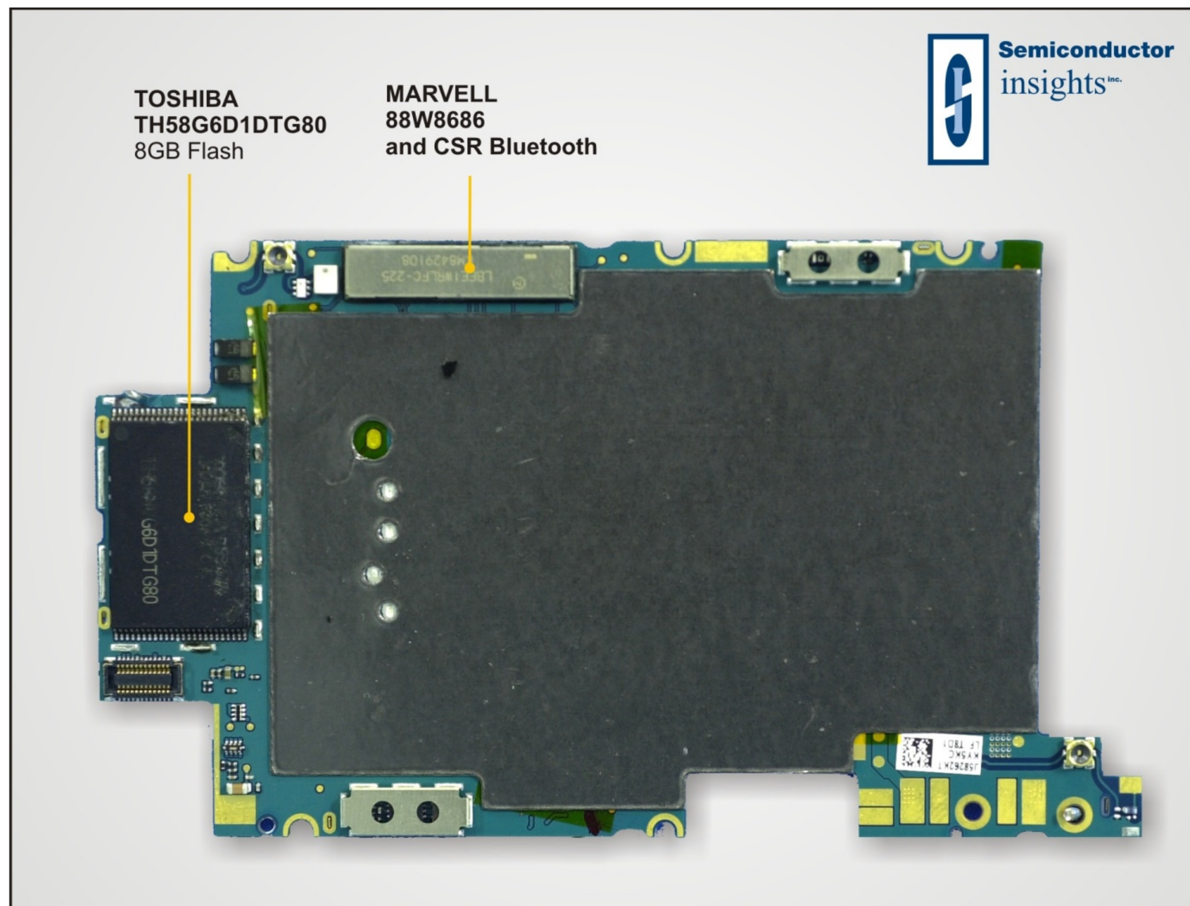
VLSI Growth

- Growth in VLSI device capabilities and speeds has made this industry exciting and dynamic
- And also beneficial to society!
  - cell phones, PCs, iPods, automobile features, etc.
- With this growth has come many issues:
  - High frequencies - difficult timing, power dissipation, reliability issues, etc.
  - Design Complexity - millions of gates, time-to-market, reliance on automation, etc.
  - Several others…

Example Design

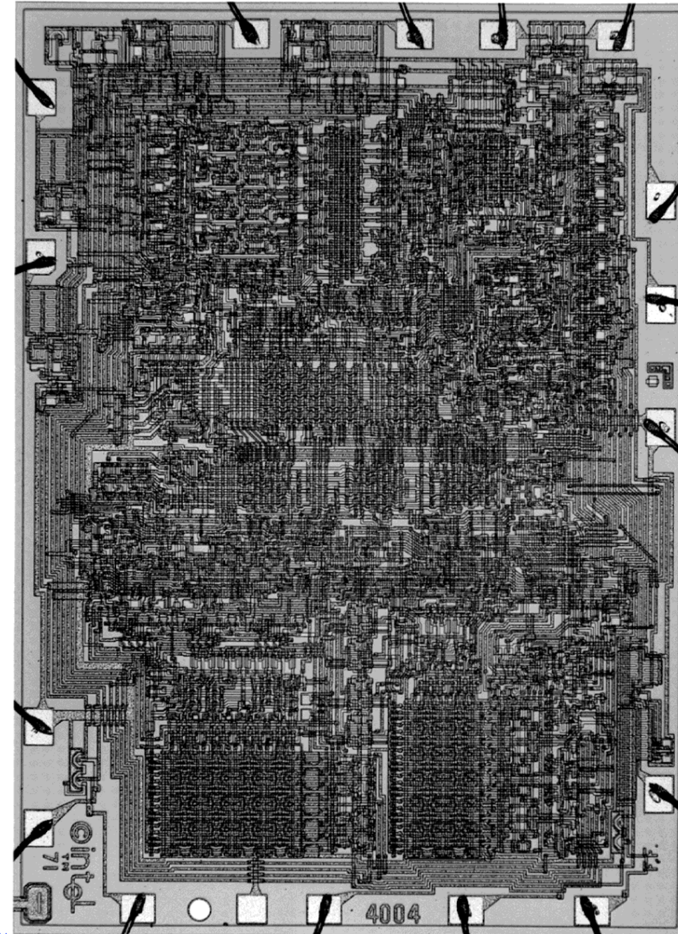


Example Design Using VLSI



Intel's First Processor

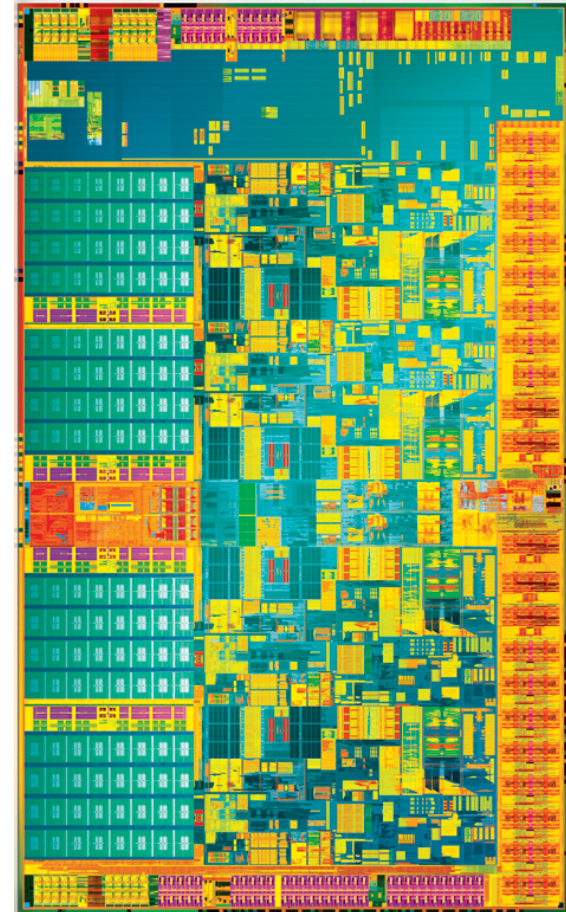
- Intel 4004 uP
  - 1971
  - 1000 transistors
  - 1 MHz operation



Source: Intel

Recent - Core i7

- Quad core (& more)
  - Pentium-style architecture
  - 2 MB L3$ / core
- Characteristics
  - 45-32 nm process
  - 731M transistors
  - 2.66-3.33+ GHz
  - Up to 130 W
  - 32/64 bit word size
  - 1366-pin LGA
  - Multithreading
- On-die memory controller



Intel uP Summary

- 10^4 increase in transistor count, clock frequency over 3 decades!

Processor	Year	Feature Size (μm)	Transistors	Frequency (MHz)	Word Size	Power (*W*)	Cache (L1 / L2 / L3)	Package
4004	1971	10	2.3k	0.75	4	0.5	none	16-pin DIP
8008	1972	10	3.5k	0.5–0.8	8	0.5	none	18-pin DIP
8080	1974	6	6k	2	8	0.5	none	40-pin DIP
8086	1978	3	29k	5–10	16	2	none	40-pin DIP
80286	1982	1.5	134k	6–12	16	3	none	68-pin PGA
Intel386	1985	1.5–1.0	275k	16–25	32	1–1.5	none	100-pin PGA
Intel486	1989	1–0.6	1.2M	25–100	32	0.3–2.5	8K	168-pin PGA
Pentium	1993	0.8–0.35	3.2–4.5M	60–300	32	8–17	16K	296-pin PGA
Pentium Pro	1995	0.6–0.35	5.5M	166–200	32	29–47	16K / 256K+	387-pin MCM PGA
Pentium II	1997	0.35–0.25	7.5M	233–450	32	17–43	32K / 256K+	242-pin SECC
Pentium III	1999	0.25–0.18	9.5–28M	450–1000	32	14–44	32K / 512K	330-pin SECC2
Pentium 4	2000	180–65 nm	42–178M	1400–3800	32/64	21–115	20K+ / 256K+	478-pin PGA
Pentium M	2003	130–90 nm	77–140M	1300–2130	32	5–27	64K / 1M	479-pin FCBGA
Core	2006	65 nm	152M	1000–1860	32	6–31	64K / 2M	479-pin FCBGA
Core 2 Duo	2006	65–45 nm	167–410M	1060–3160	32/64	10–65	64K / 4M+	775-pin LGA
Core i7	2008	45 nm	731M	2660–3330	32/64	45–130	64K / 256K / 8M	1366-pin LGA
Atom	2008	45 nm	47M	800–1860	32/64	1.4–13	56K / 512K+	441-pin FCBGA

Slowing Clock Increases

10000.00
1000.00
100.00
10.00
1.00

Relative Performance

Historical
+IPC
+Pipelining
Technology

GAP

8-10 FO4
Pipeline

Pipelining

Semiconductor
Technology

40x
6.6x
10x

1996 1998 2000 2002 2004 2006 2008 2010 2012 2014

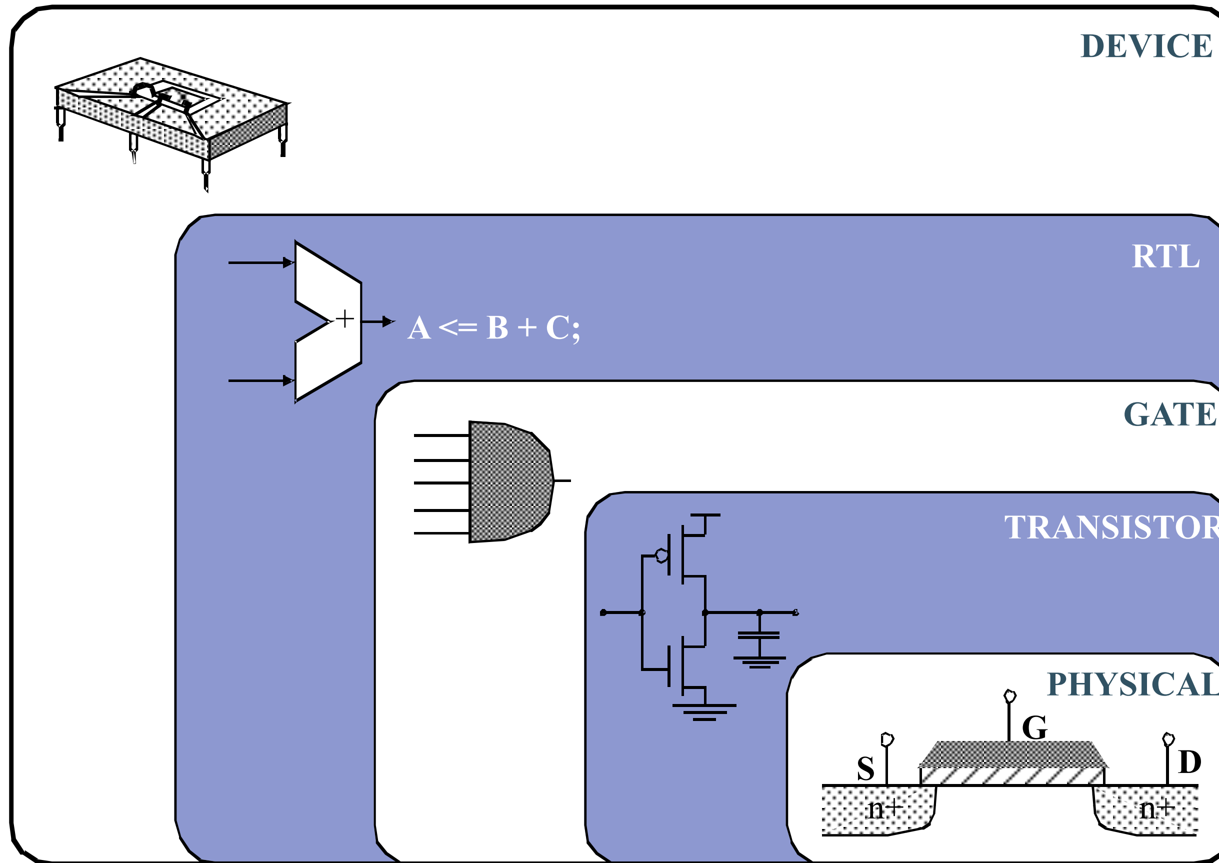
Source: UT Dept. Computer Science

Semiconductor, Inc. 2006. 4

So many transistors…

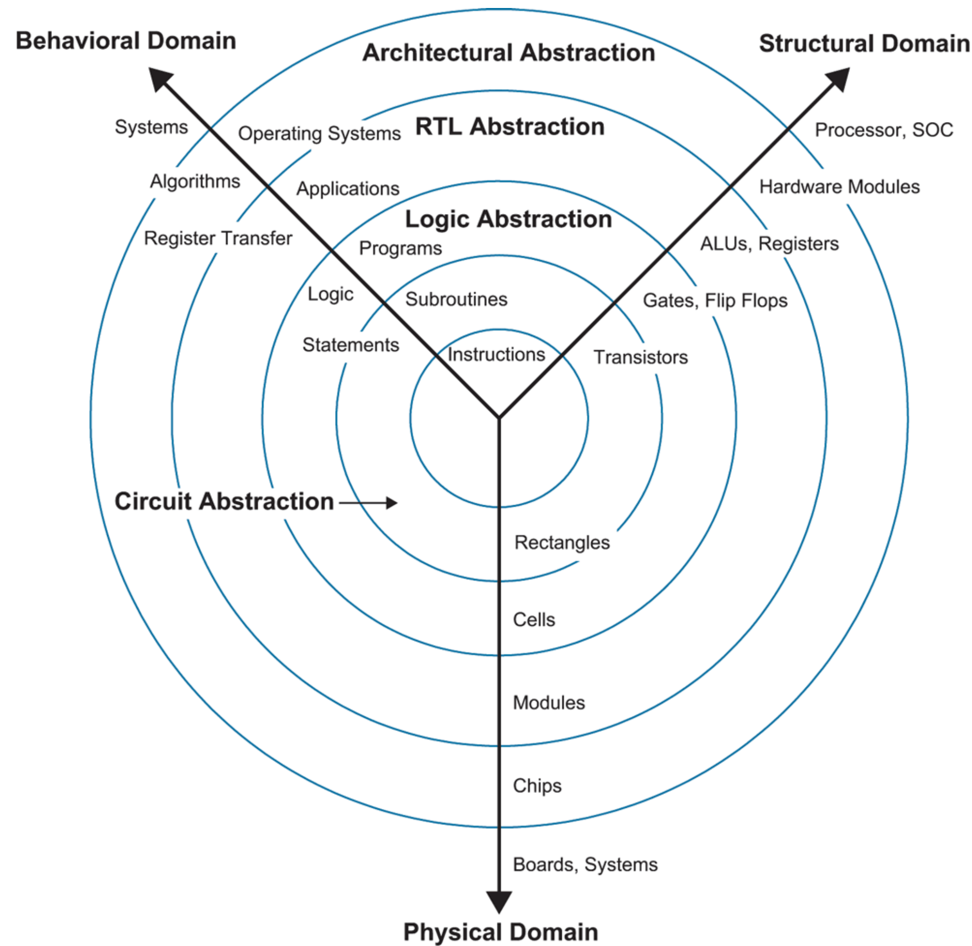
- Technology shrinks by 0.7/generation
- Each generation can integrate 2x more functions per chip; while chips cost about the same
- Cost of a function decreases by 2x
- But …
  - How to design chips with more and more functions?
  - Design engineering population does not double every two years…
- Hence, a need for more efficient design methods
  - Exploit different levels of abstraction

Levels of Abstraction



Adapted from "Digital Integrated Circuits" copyright 2003 Prentice Hall/Pearson

Levels of Abstraction

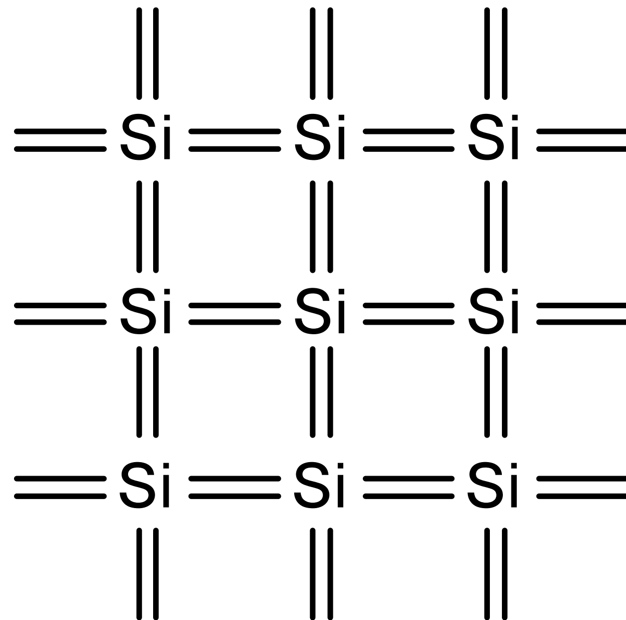


Various VLSI Jobs

- Architect
- Performance analysis
- RTL design
- Synthesis
- Test insertion
- Layout
- Signal Integrity
- Verification
- Common characteristic – Attention to detail!

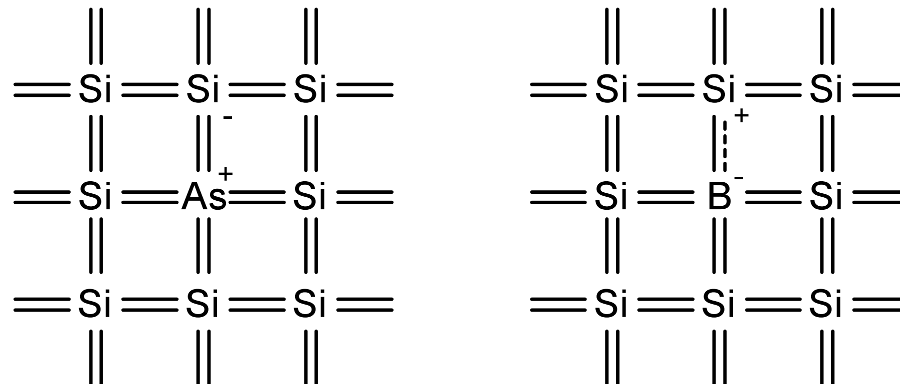
Silicon Lattice

- Transistors are built on a silicon substrate
- Silicon is a Group IV material
- Forms crystal lattice with bonds to four neighbors



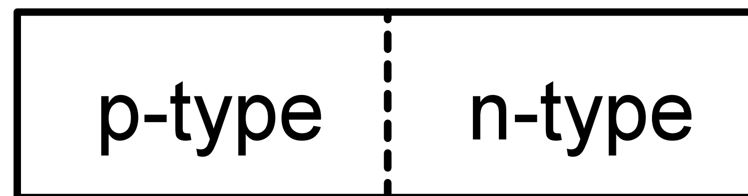
Dopants

- Silicon is a semiconductor
- Pure silicon has no free carriers and conducts poorly
- Adding dopants increases the conductivity
- Group V: extra electron (n-type)
- Group III: missing electron, called hole (p-type)

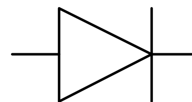


p-n Junctions

- A junction between p-type and n-type semiconductor forms a diode.
- Current flows only in one direction

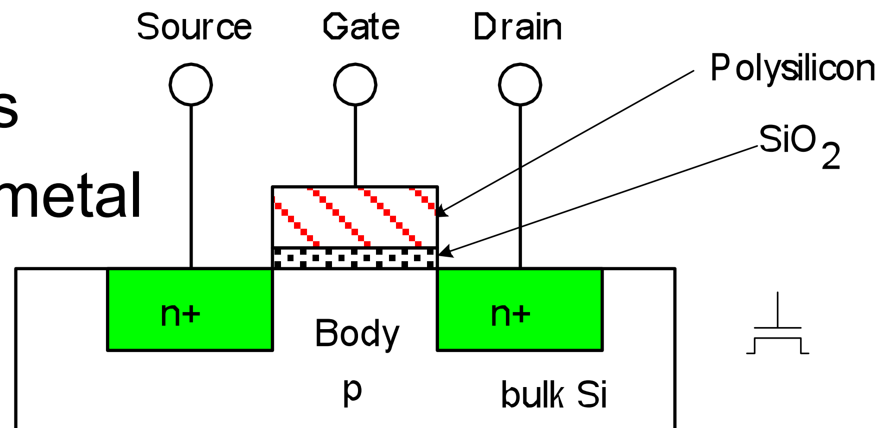


anode cathode



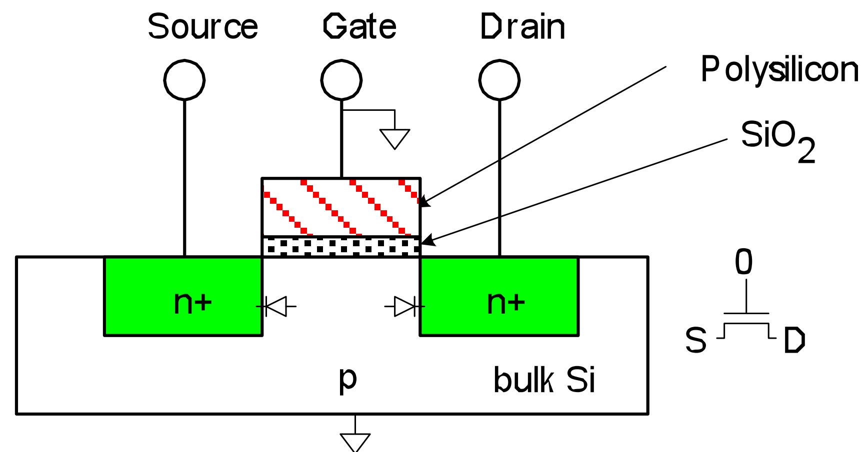
nMOS Transistor

- Four terminals: gate, source, drain, body
- Gate – oxide – body stack looks like a capacitor
  - Gate and body are conductors
  - SiO_2 (oxide) is a very good insulator
  - Called metal – oxide – semiconductor (MOS) capacitor
  - Even though gate is no longer made of metal



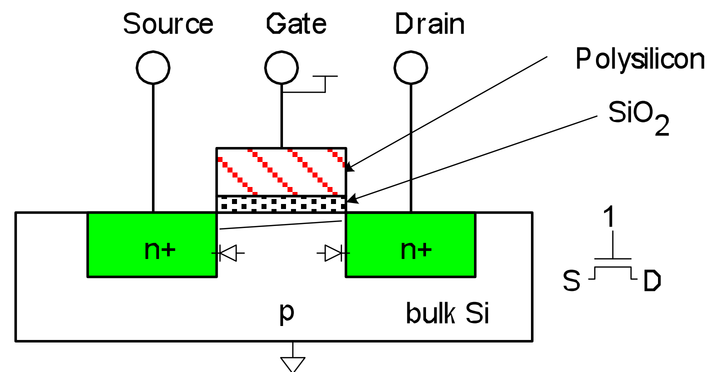
nMOS Operation

- Body is usually tied to ground (0 V)
- When the gate is at a low voltage:
  - P-type body is at low voltage
  - Source-body and drain-body diodes are OFF
  - No current flows, transistor is OFF



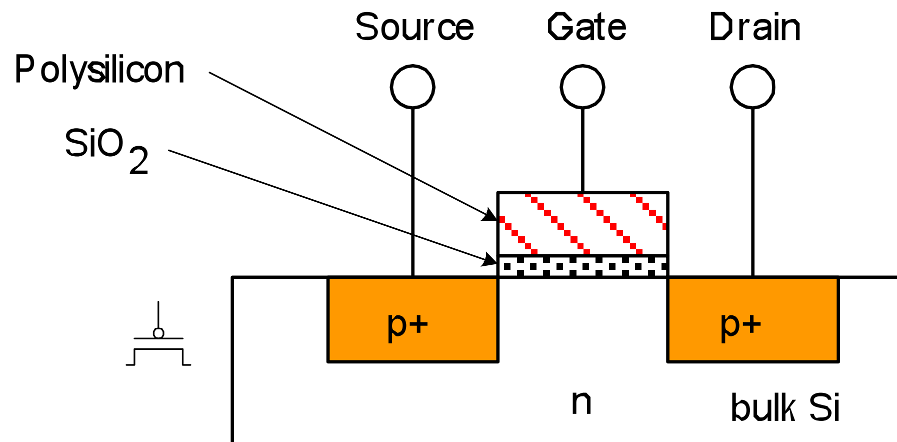
nMOS Operation Cont.

- When the gate is at a high voltage:
  - Positive charge on gate of MOS capacitor
  - Negative charge attracted to body
  - Inverts a channel under gate to n-type
  - Now current can flow through n-type silicon from source through channel to drain, transistor is ON



pMOS Transistor

- Similar, but doping and voltages reversed
  - Body tied to high voltage (V_{DD})
  - Gate low: transistor ON
  - Gate high: transistor OFF
  - Bubble indicates inverted behavior

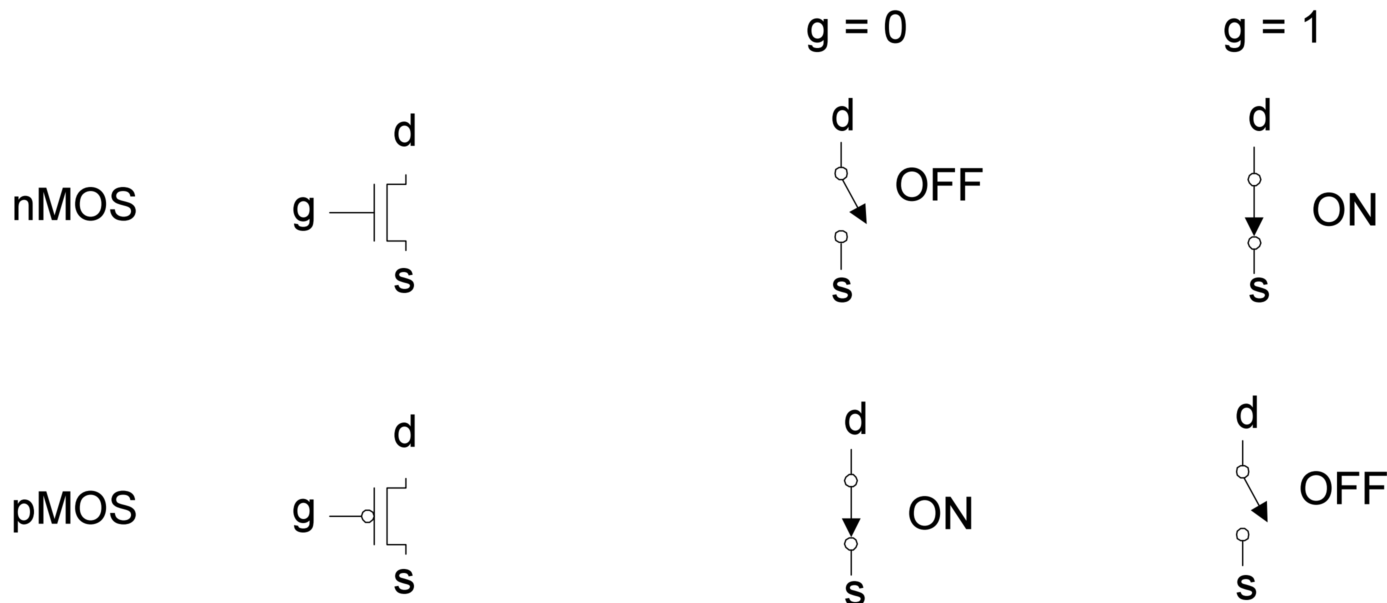


Power Supply Voltage

- GND = 0 V
- In 1980's, V_{DD} = 5V
- V_{DD} has decreased in modern processes
  - High V_{DD} would damage modern tiny transistors
  - Lower V_{DD} saves power
- V_{DD} = 3.3, 2.5, 1.8, 1.5, 1.2, 1.0, …

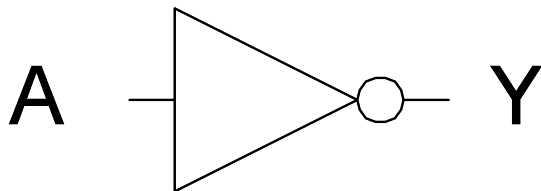
Transistors as Switches

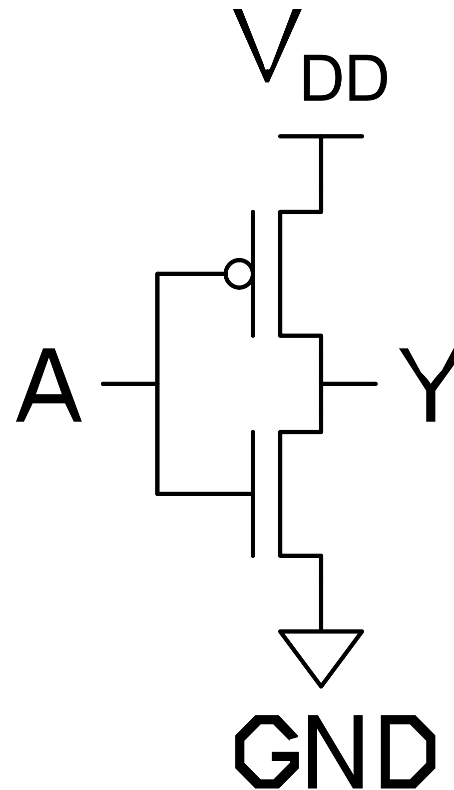
- We can view MOS transistors as electrically controlled switches
- Voltage at gate controls path from source to drain



CMOS Inverter

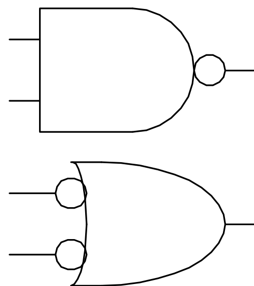
A	Y

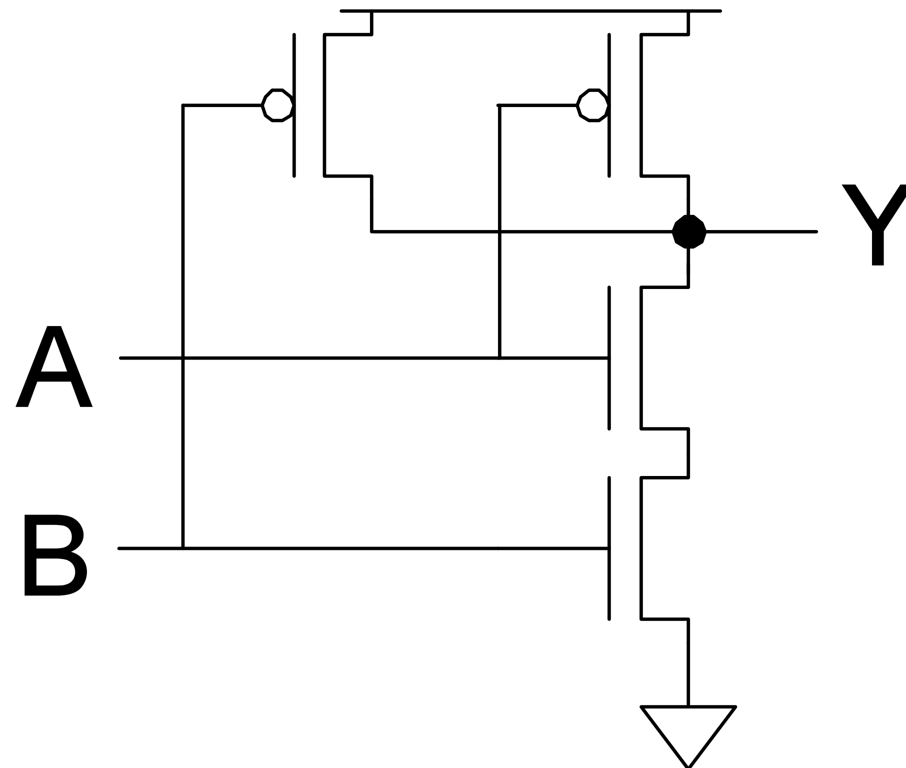




CMOS NAND Gate

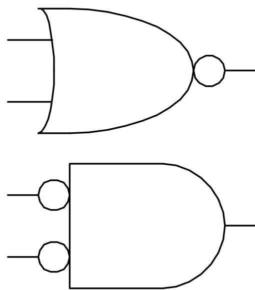
A	B	Y
0	0	
0	1	
1	0	
1	1	

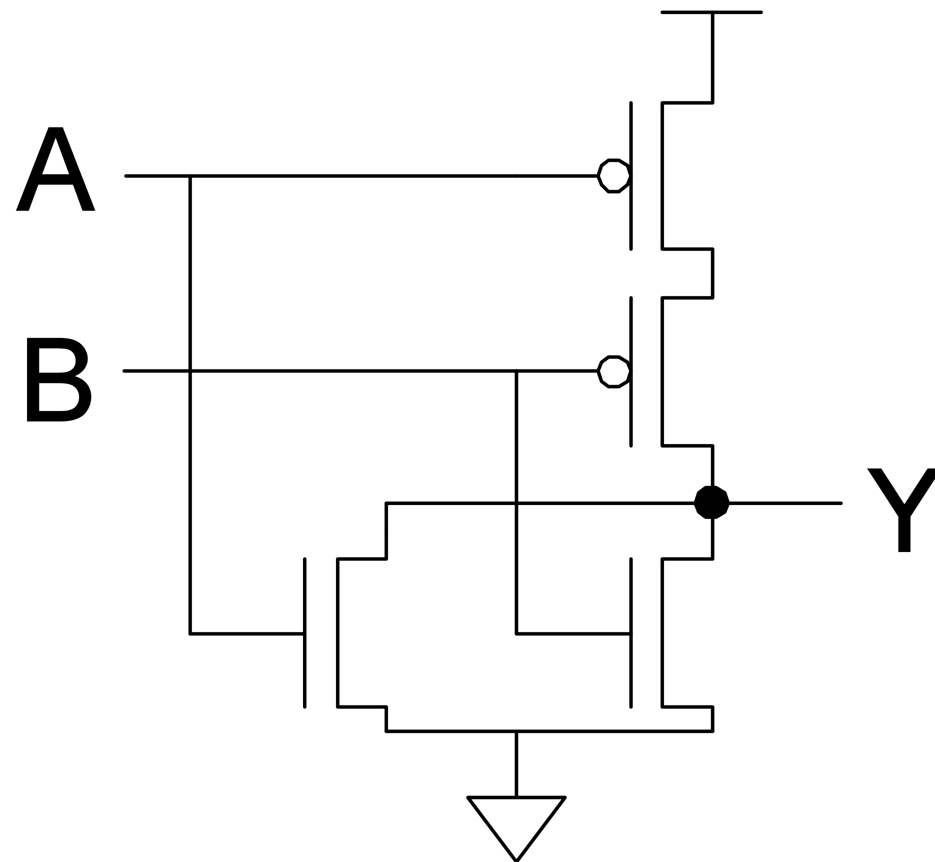




CMOS NOR Gate

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0





3-input NAND Gate

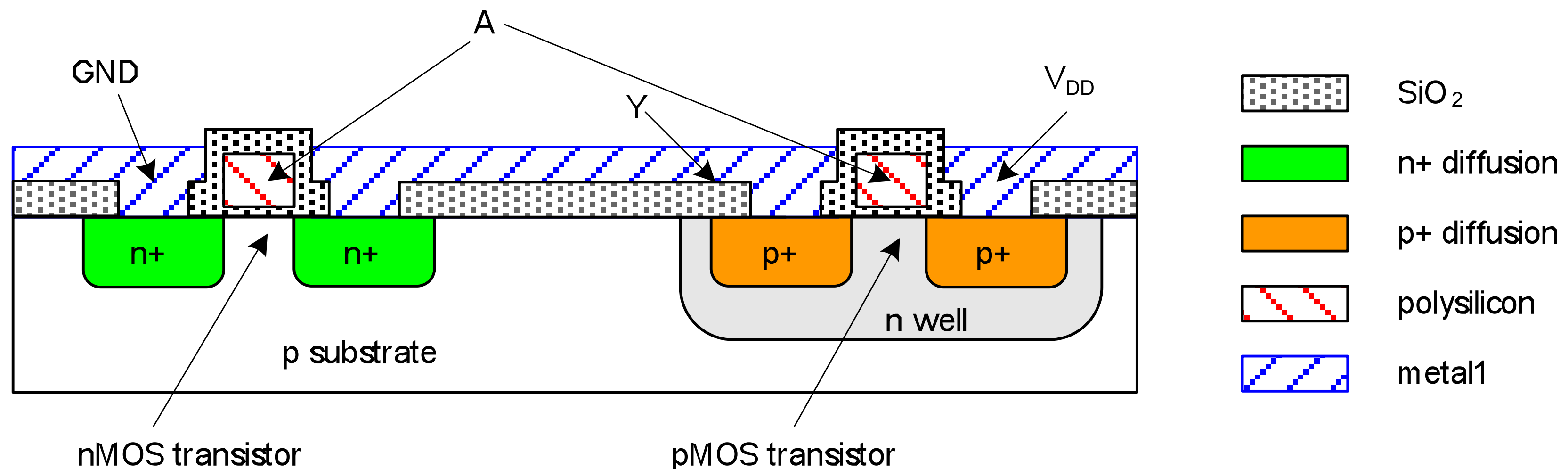
- Y pulls low if ALL inputs are 1
- Y pulls high if ANY input is 0

CMOS Fabrication

- CMOS transistors are fabricated on silicon wafer
- Lithography process similar to printing press
- On each step, different materials are deposited or etched
- Easiest to understand by viewing both top and cross-section of wafer in a simplified manufacturing process

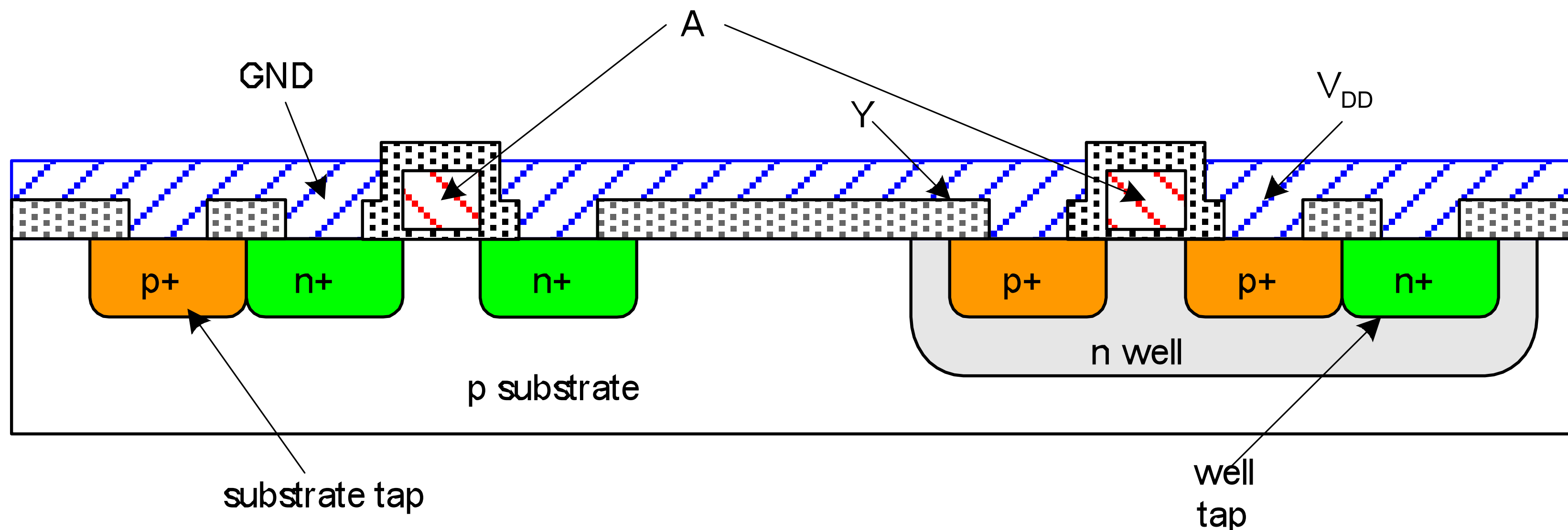
Inverter Cross-section

- Typically use p-type substrate for nMOS transistors
- Requires n-well for body of pMOS transistors



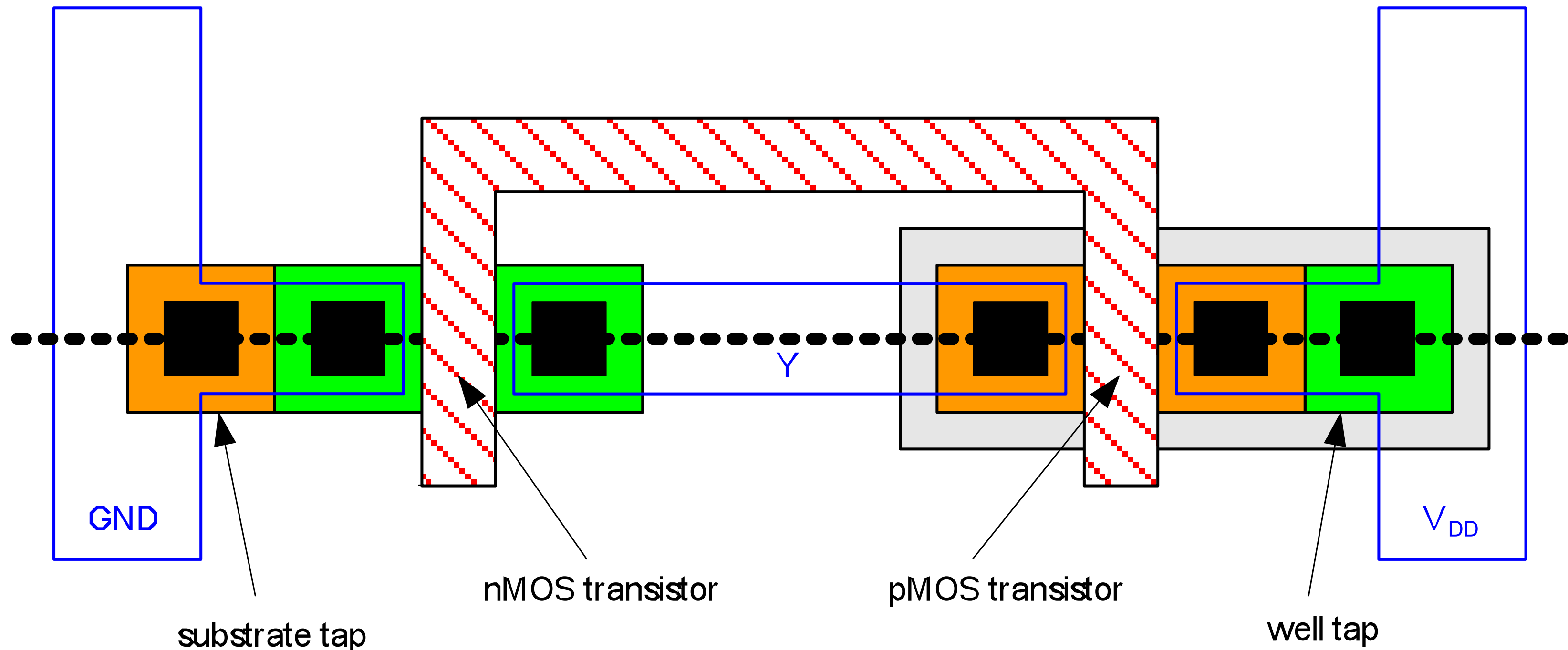
Well and Substrate Taps

- Substrate must be tied to GND and n-well to V_{DD}
- Metal to lightly-doped semiconductor forms poor connection called Shottky Diode
- Use heavily doped well and substrate contacts / taps



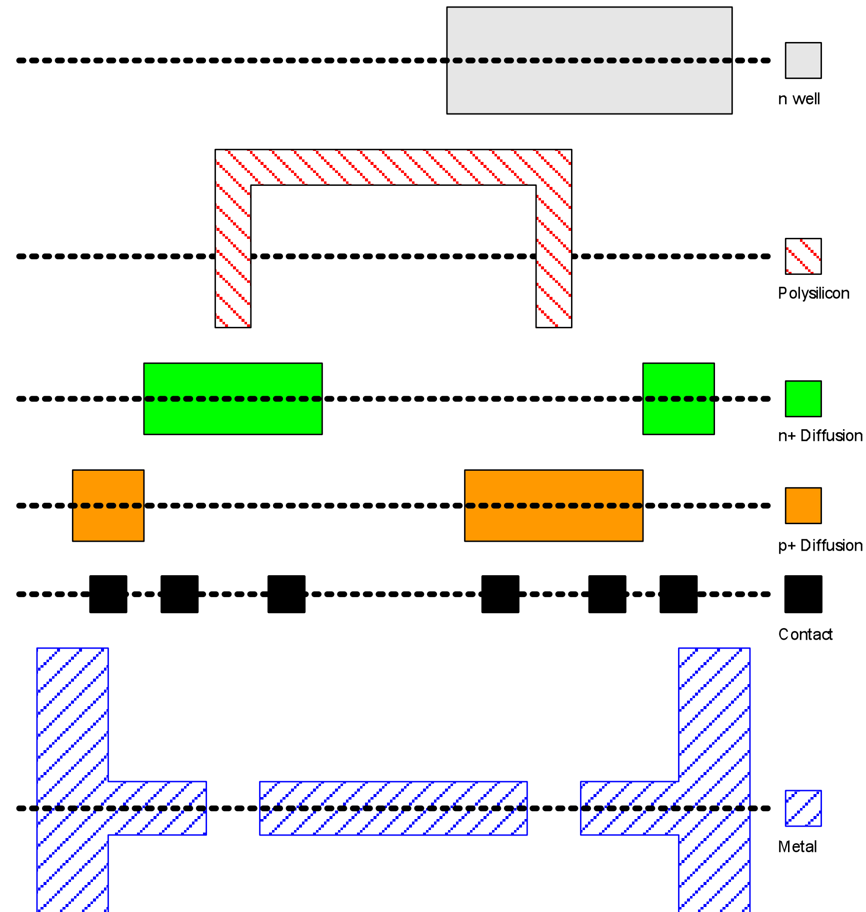
Inverter Mask Set

- Transistors and wires are defined by *masks*
- Cross-section taken along dashed line



Detailed Mask Views

- Six masks
  - n-well
  - Polysilicon
  - n+ diffusion
  - p+ diffusion
  - Contact
  - Metal



Fabrication

- Chips are built in huge factories called fabs
- Contain clean rooms as large as football fields

Courtesy of International
Business Machines Corporation.
Unauthorized use not permitted.

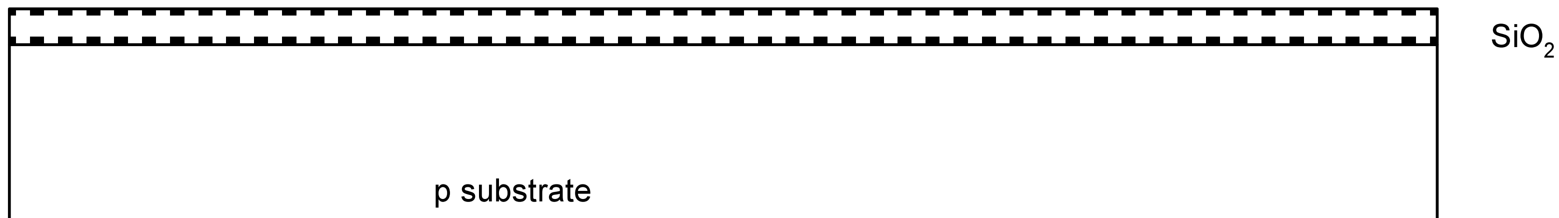
Fabrication Steps

- Start with blank wafer
- Build inverter from the bottom up
- First step will be to form the n-well
  - Cover wafer with protective layer of SiO_2 (oxide)
  - Remove layer where n-well should be built
  - Implant or diffuse n dopants into exposed wafer
  - Strip off SiO_2

p substrate

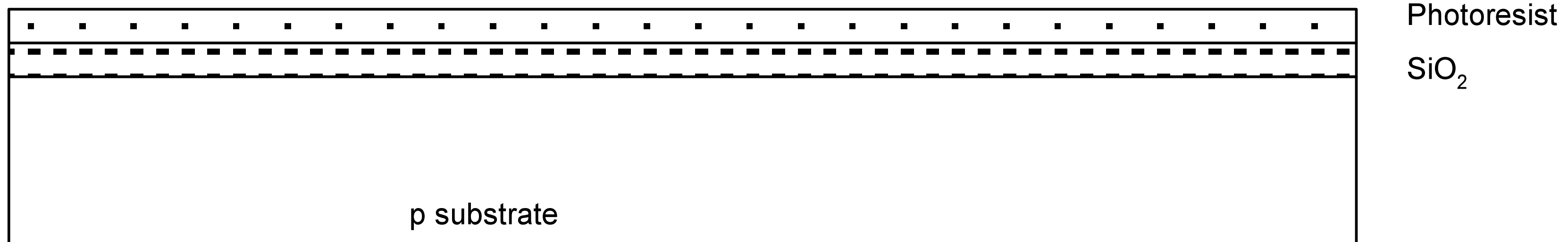
Oxidation

- Grow SiO_2 on top of Si wafer
  - 900 – 1200 C with H_2O or O_2 in oxidation furnace



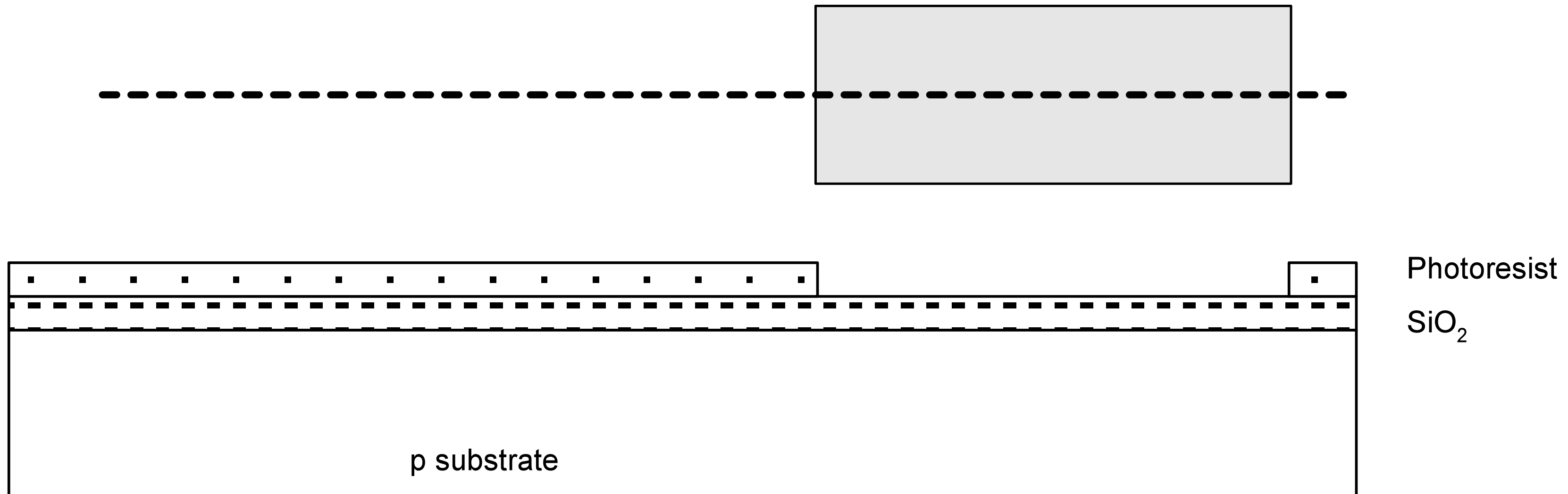
Photoresist

- Spin on photoresist
  - Photoresist is a light-sensitive organic polymer
  - Softens where exposed to light



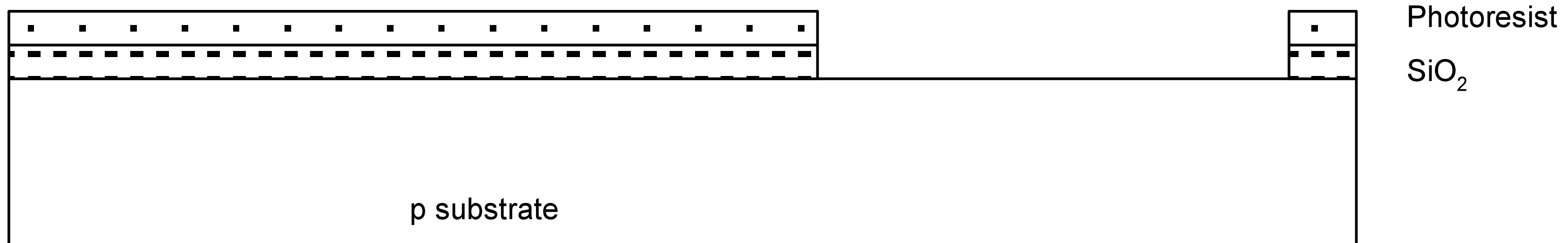
Lithography

- Expose photoresist through n-well mask
- Strip off exposed photoresist



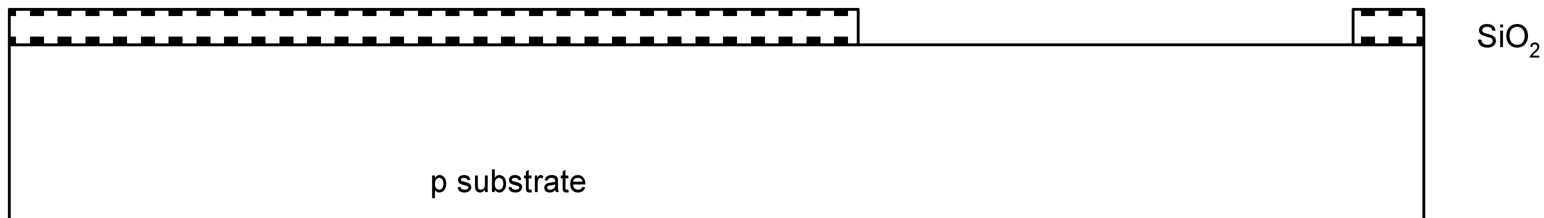
Etch

- ❑ Etch oxide with hydrofluoric acid (HF)
  - – Seeps through skin and eats bone; nasty stuff!!!
- ❑ Only attacks oxide where resist has been exposed



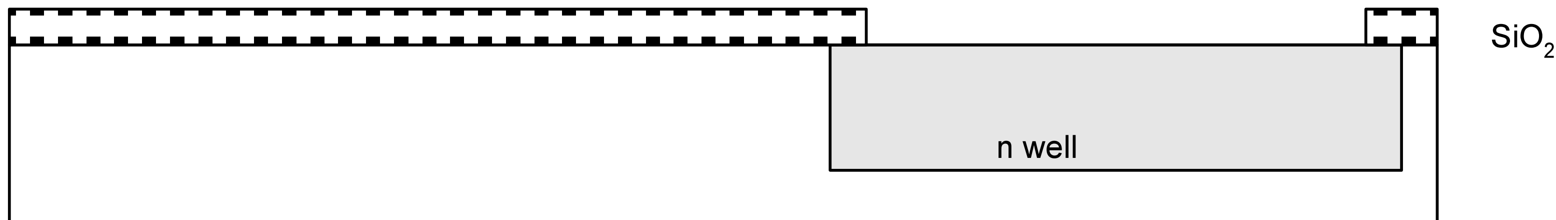
Strip Photoresist

- Strip off remaining photoresist
  - Use mixture of acids called piranah etch
- Necessary so resist doesn't melt in next step



n-well

- n-well is formed with diffusion or ion implantation
- Diffusion
  - Place wafer in furnace with arsenic gas
  - Heat until As atoms diffuse into exposed Si
- Ion Implanatation
  - Blast wafer with beam of As ions
  - Ions blocked by SiO_2, only enter exposed Si

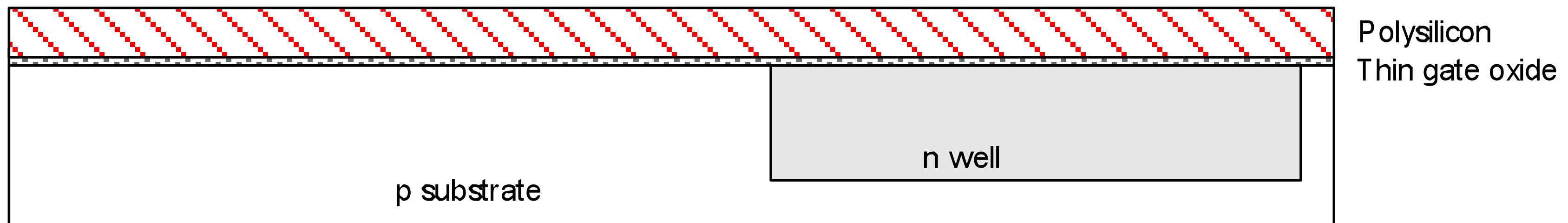


Strip Oxide

- Strip off the remaining oxide using HF
- Back to bare wafer with n-well
- Subsequent steps involve similar series of steps

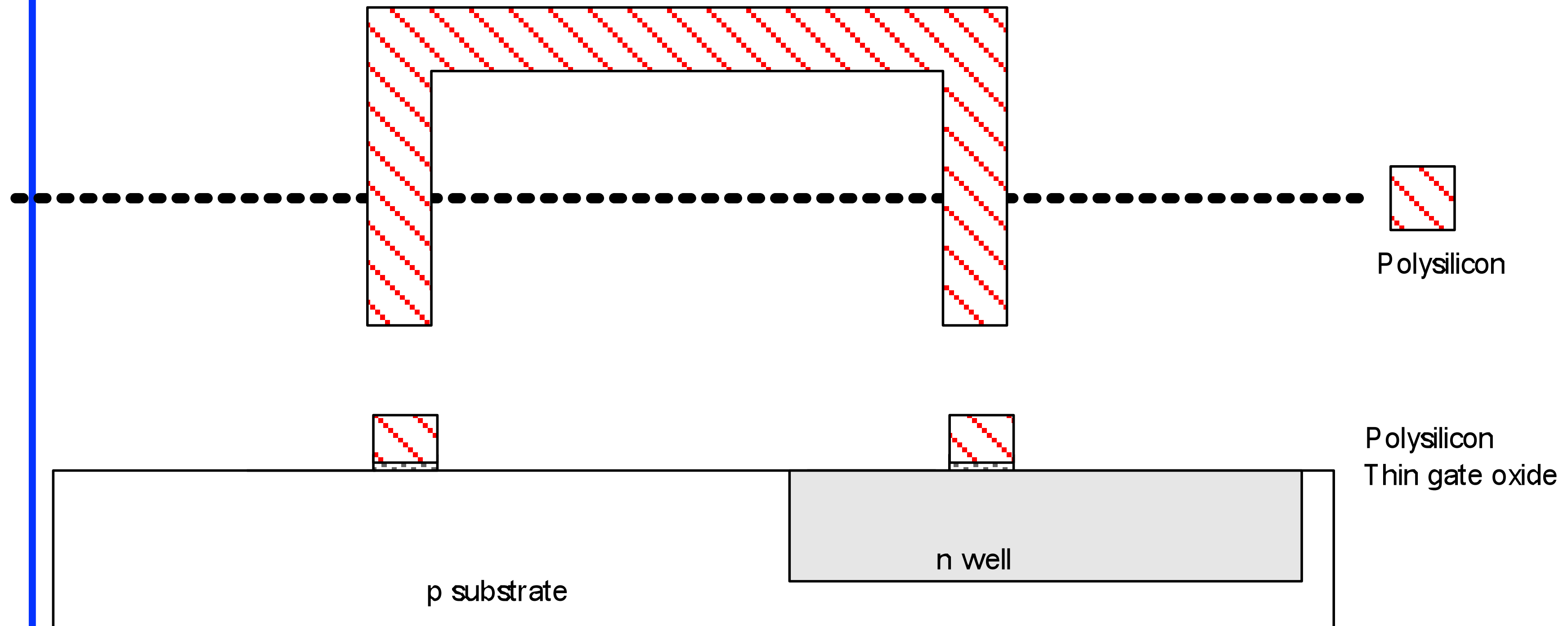
Polysilicon

- Deposit very thin layer of gate oxide
  - < 20 Å (6-7 atomic layers)
- Chemical Vapor Deposition (CVD) of silicon layer
  - Place wafer in furnace with Silane gas (SiH_4)
  - Forms many small crystals called polysilicon
  - Heavily doped to be good conductor



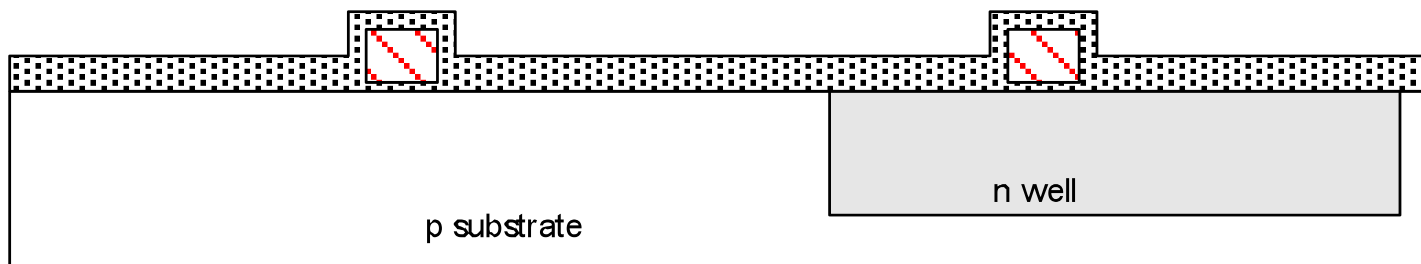
Polysilicon Patterning

- Use same lithography process to pattern polysilicon



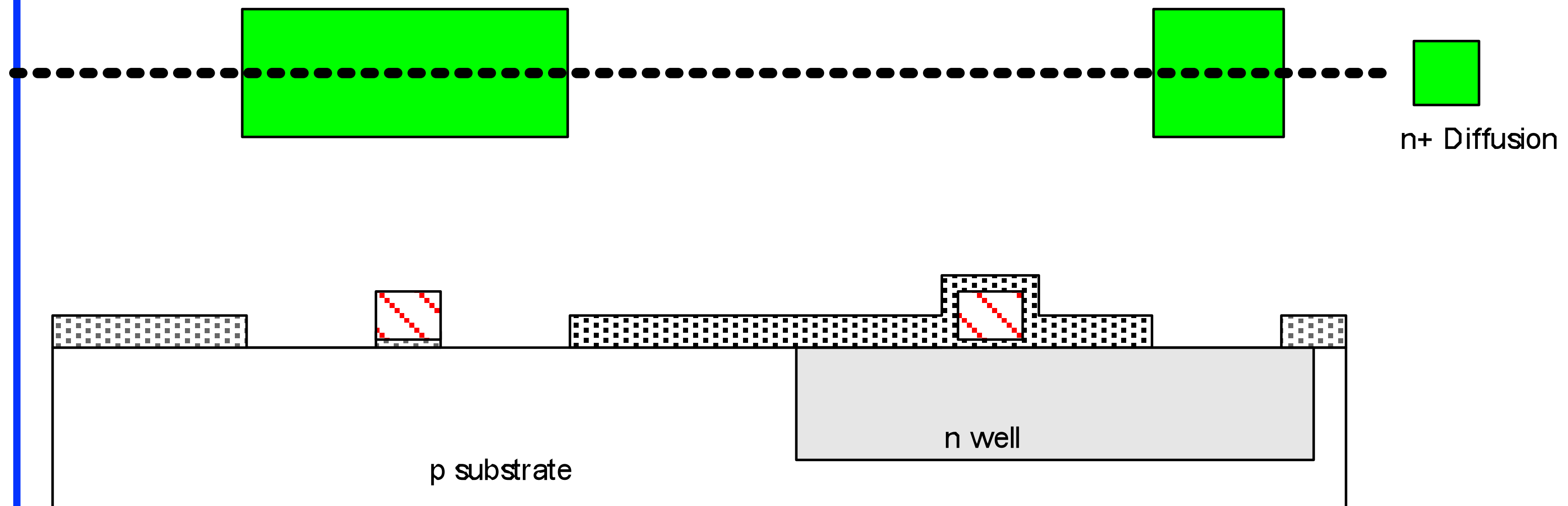
Self-Aligned Process

- Use oxide and masking to expose where n+ dopants should be diffused or implanted
- N-diffusion forms nMOS source, drain, and n-well contact



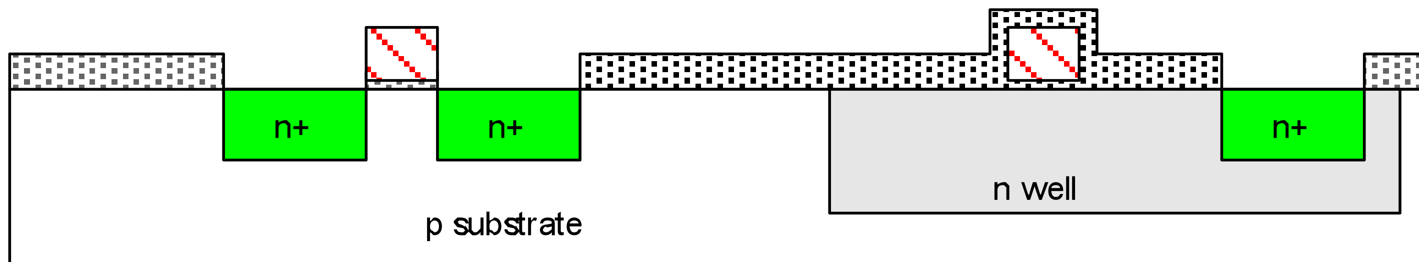
N-diffusion

- Pattern oxide and form n+ regions
- *Self-aligned process* where gate blocks diffusion
- Polysilicon is better than metal for self-aligned gates because it doesn't melt during later processing



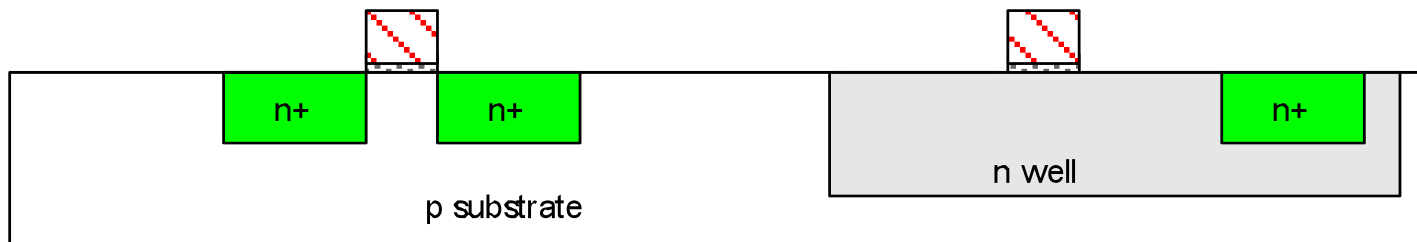
N-diffusion cont.

- Historically dopants were diffused
- Usually ion implantation today
- But regions are still called diffusion



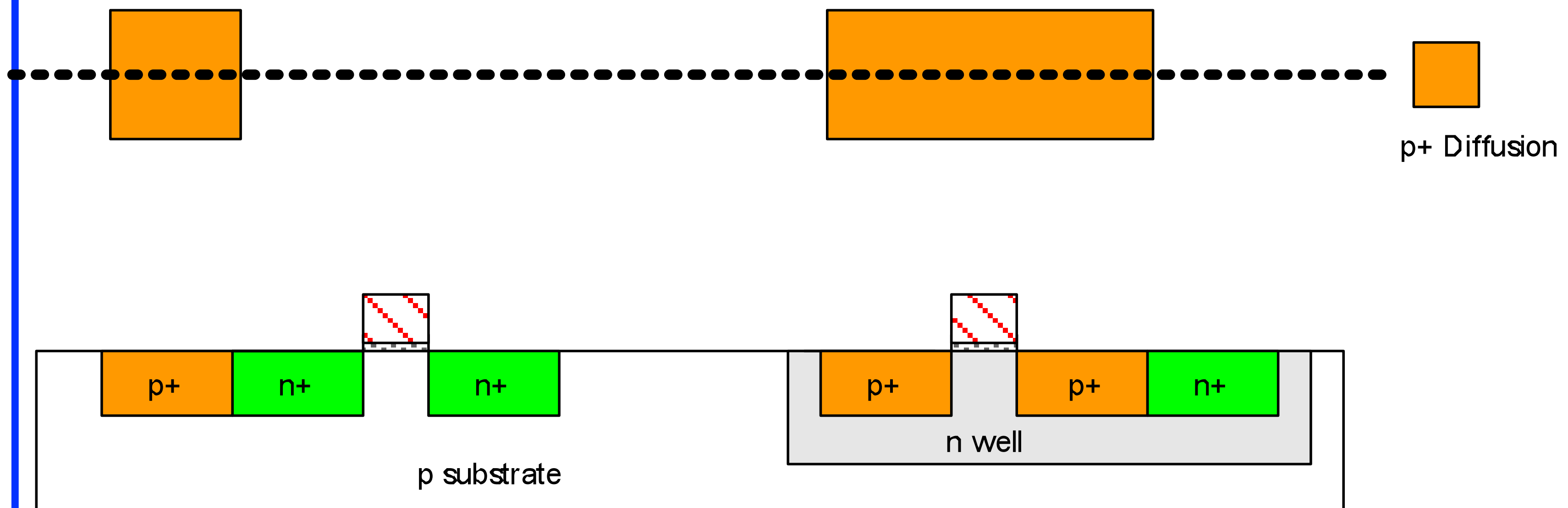
N-diffusion cont.

- Strip off oxide to complete patterning step



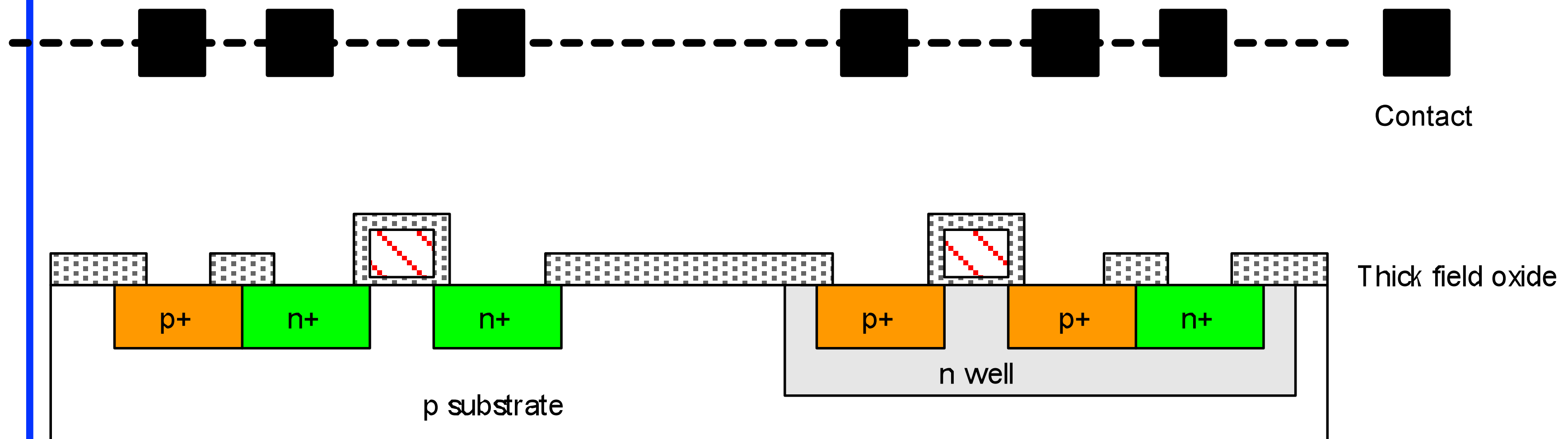
P-Diffusion

- Similar set of steps form p+ diffusion regions for pMOS source and drain and substrate contact



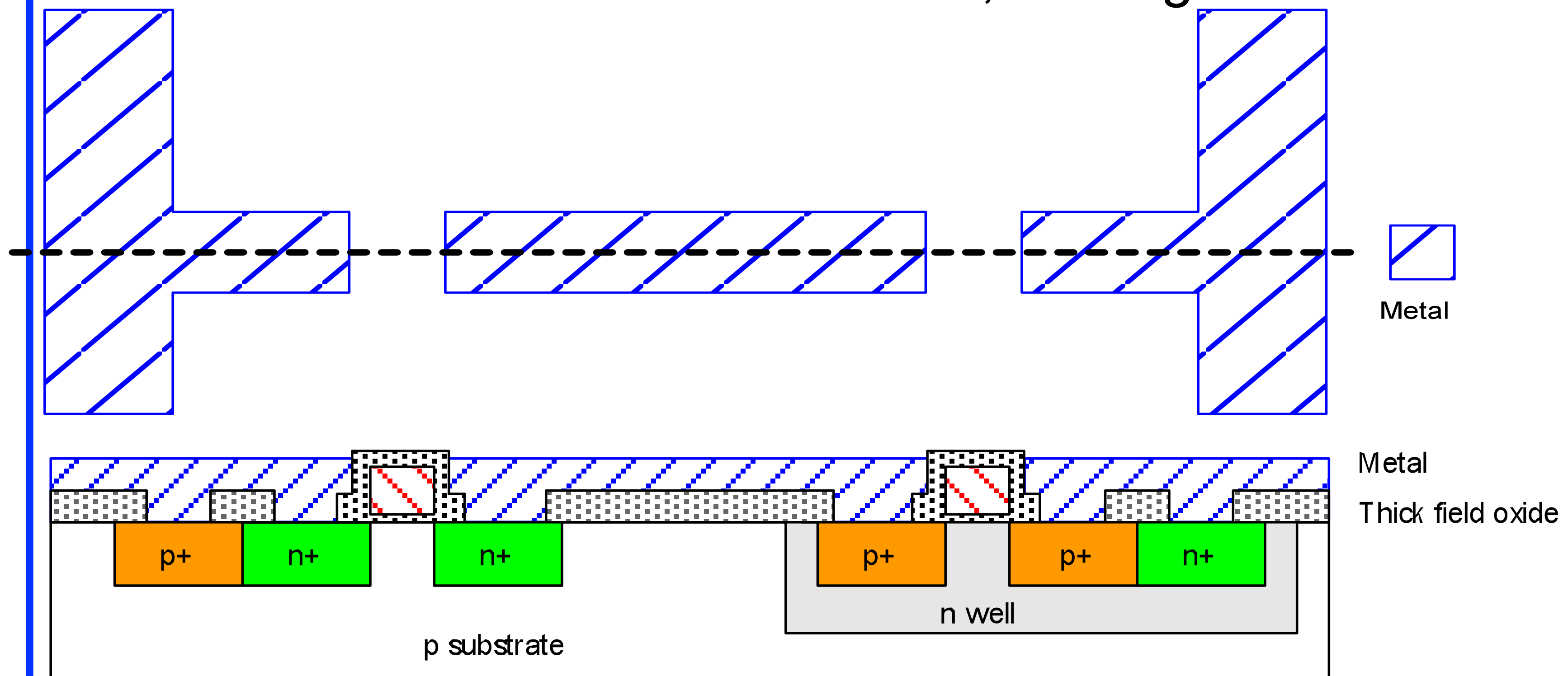
Contacts

- Now we need to wire together the devices
- Cover chip with thick field oxide
- Etch oxide where contact cuts are needed



Metalization

- Sputter on aluminum over whole wafer
- Pattern to remove excess metal, leaving wires

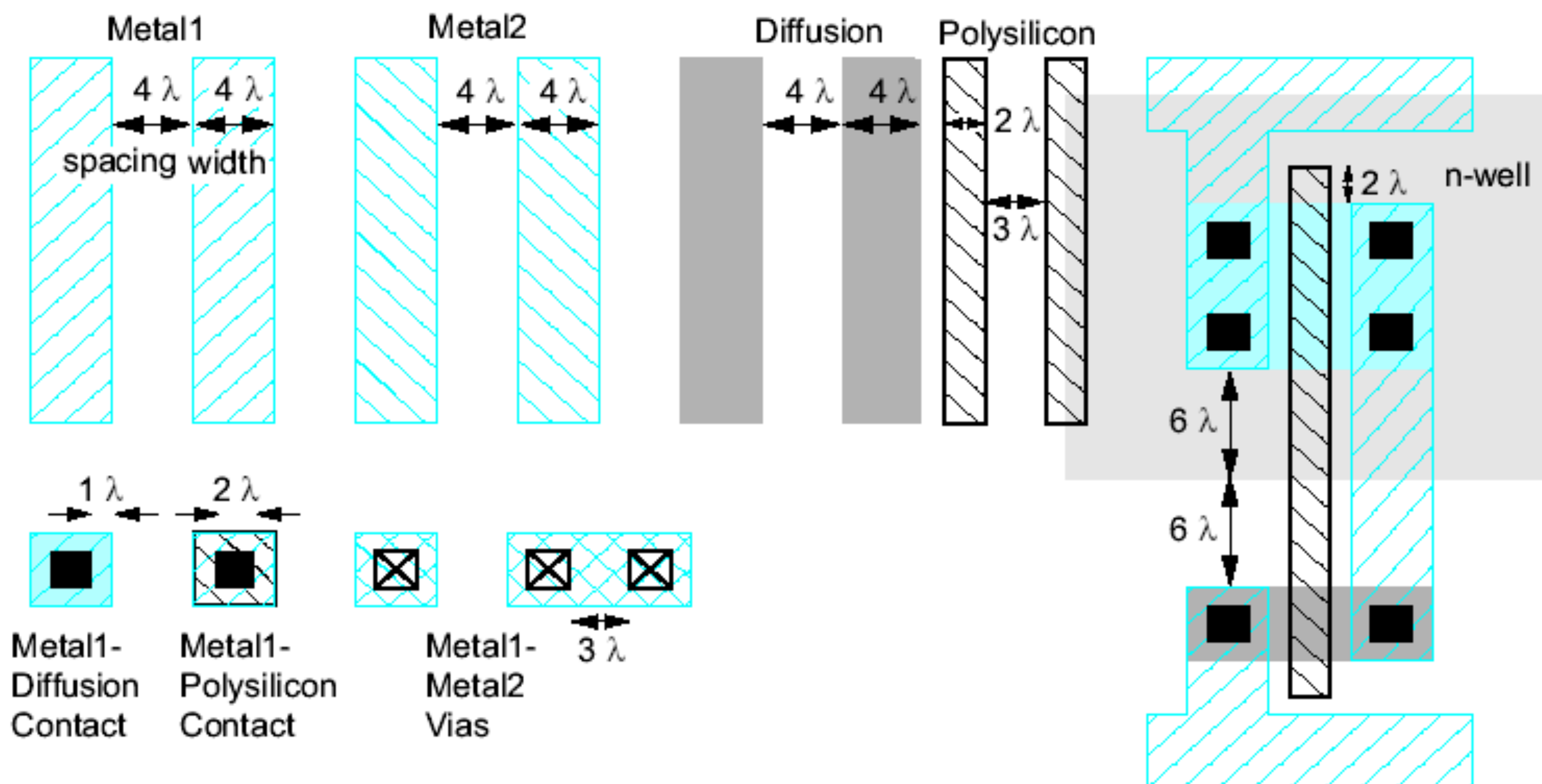


Layout

- Chips are specified with set of masks
- Minimum dimensions of masks determine transistor size (and hence speed, cost, and power)
- Feature size *f* = distance between source and drain
  - Set by minimum width of polysilicon
- Feature size improves 30% every 3 years or so
- Normalize for feature size when describing design rules
- Express rules in terms of $\lambda = f/2$
  - E.g. λ = 0.3 μm in 0.6 μm process

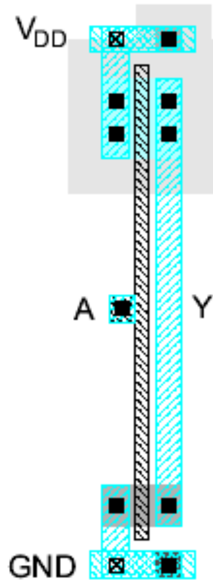
Simplified Design Rules

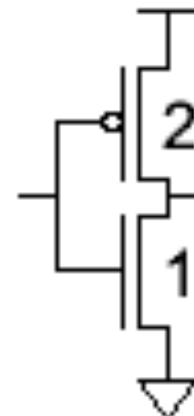
- Conservative rules to get you started



Inverter Layout

- Transistor dimensions specified as Width / Length
  - Minimum size is $4\lambda / 2\lambda$, sometimes called 1 unit
  - In f = 0.6 μm process, this is 1.2 μm wide, 0.6 μm long





Summary

- MOS transistors are stacks of gate, oxide, silicon
- Act as electrically controlled switches
- Build logic gates out of switches
- Draw masks to specify layout of transistors
- Now you know everything necessary to start designing a schematic and layout for a simple chip