Flash and DRAM
Adapted from Weste and Harris notes except as noted
Flash and DRAM sections adapted from “Digital Integrated Circuits”, copyright 2003 Prentice Hall/ Pearson
Outline

- Memory Arrays
- Flash
- DRAM
Memory Arrays

Random Access Memory
- Read/Write Memory (RAM) (Volatile)
  - Static RAM (SRAM)
  - Dynamic RAM (DRAM)
- Read Only Memory (ROM) (Nonvolatile)
  - Mask ROM
  - Programmable ROM (PROM)
  - Erasable Programmable ROM (EPROM)
  - Electrically Erasable Programmable ROM (EEPROM)

Serial Access Memory
- Serial In Parallel Out (SIPO)
- Parallel In Serial Out (PISO)

Content Addressable Memory (CAM)
- Shift Registers
- Queues
  - First In First Out (FIFO)
  - Last In First Out (LIFO)

Flash ROM
Array Architecture

- $2^n$ words of $2^m$ bits each
- If $n >> m$, fold by $2^k$ into fewer rows of more columns

- Good regularity – easy to design
- Very high density if good cells are used
Non-Volatile Memories

- Floating-gate transistor

Device cross-section

Schematic symbol
Floating-Gate Transistor Programming

\[ \begin{align*}
&0 \text{ V} & & 20 \text{ V} & & 20 \text{ V} & & 20 \text{ V} & & 10 \text{ V} \\
&20 \text{ V} & & 20 \text{ V} & & 0 \text{ V} & & 8 \text{ V} & & ? \text{ V} \\
\text{Erase} & & \text{Inhibit} & & \text{Erase} & & \text{Program 0} & & \text{Do Not} & & \text{Program} \\
\end{align*} \]

FN Tunneling
Remove e-
Negative Vt
“1”

FN Tunneling
Add e-
Positive Vt
“0”
NAND Flash Memory

Word line (poly)

Unit Cell

Source line (Diff. Layer)

Courtesy Toshiba
NAND Flash Memory

Select transistor

Word lines

Active area

STI

Bit line contact

Source line contact

Courtesy Toshiba
Read-Write Memories (RAM)

- Static (SRAM)
  - Data stored as long as supply is applied
  - Large (6 transistors/cell)
  - Fast
  - Differential

- Dynamic (DRAM)
  - Periodic refresh required
  - Small (1-3 transistors/cell)
  - Slower
  - Single Ended
3-Transistor DRAM Cell

- No constraints on device ratios
- Reads are non-destructive
- Value stored at node X when writing a “1” = $V_{\text{wwl}} - V_{\text{tn}}$
3T-DRAM — Layout
1-Transistor DRAM Cell

- **Write**: Cs is charged or discharged by asserting WL and BL
- **Read**: Charge redistribution takes place between bit line and storage capacitance
- **Voltage swing is small**: typically around 250 mV
DRAM Cell Observations

- 1T DRAM requires a sense amplifier for each bit line, due to charge redistribution read-out.
- DRAM memory cells are single ended in contrast to SRAM cells.
- The read-out of the 1T DRAM cell is destructive; read and refresh operations are necessary for correct operation.
- Unlike 3T cell, 1T cell requires presence of an extra capacitance that must be explicitly included in the design.
- When writing a “1” into a DRAM cell, a threshold voltage is lost. This charge loss can be circumvented by bootstrapping the word lines to a higher value than $V_{DD}$. 

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Sense Amp Operation

\[ \Delta V \]

\[ V(1) \]

\[ V(0) \]

\[ V_{\text{PRE}} \]

\[ V_{\text{BL}} \]

Sense amp activated

Word line activated

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1-T DRAM Cell

Uses Polysilicon-Diffusion Capacitance
Expensive in Area
Advanced 1T DRAM Cells

Trench Cell

Stacked-capacitor Cell

Cell Plate Si
Capacitor Insulator
Storage Node Poly
2nd Field Oxide

Word line
Insulating Layer
Capacitor dielectric layer

Cell plate
Transfer gate
Isolation
Storage electrode

Refilling Poly
Si Substrate
DRAM Timing

Addresses

Row Address

Column Address

W (Data out)

High Z

Valid data

\[ V_{IH} \quad V_{IL} \]

\[ t_{ASR} \]

\[ t_{RH} \]

\[ t_{RCS} \]

\[ t_{AA} \]

\[ t_{CAC} \]

\[ t_{CL} \]

\[ t_{OFF} \]
Redundancy

- Redundant rows
- Redundant columns
- Memory Array
- Row Decoder
- Column Decoder
- Row Address
- Column Address
- Fuse Bank