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Introduction to VLSI Design

Flash and DRAM

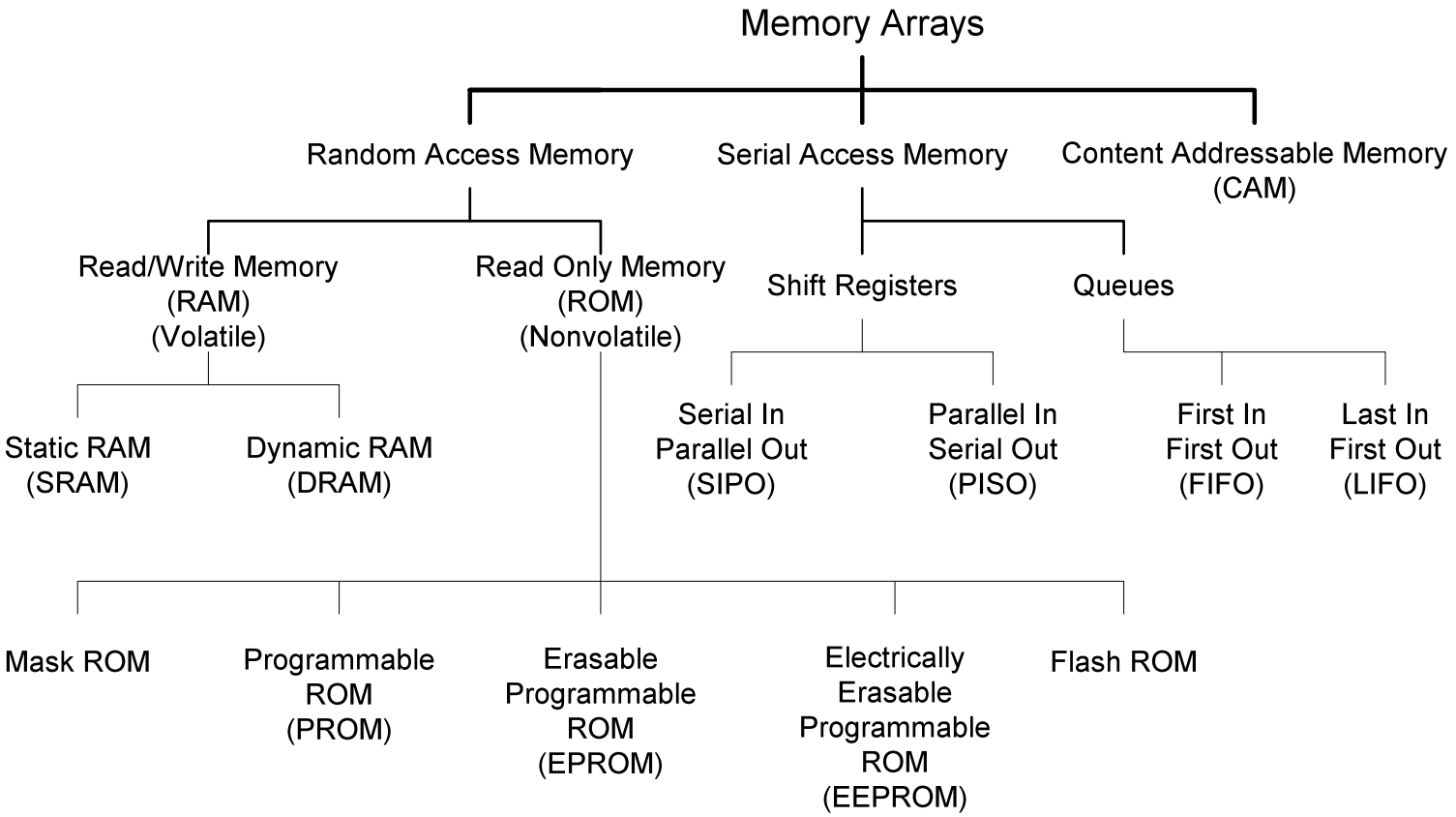
Adapted from Weste and Harris notes except as noted

Flash and DRAM sections adapted from “Digital Integrated Circuits”, copyright 2003 Prentice Hall/ Pearson

Outline

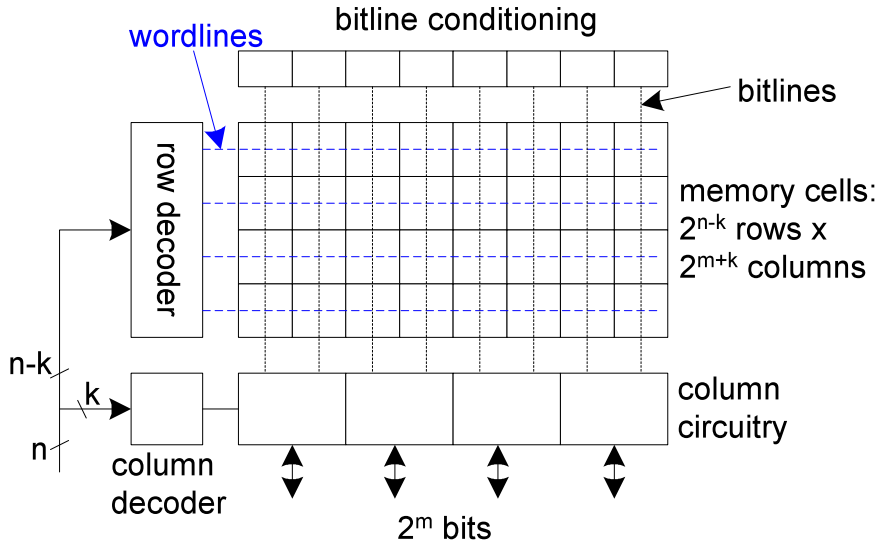
- Memory Arrays
- Flash
- DRAM

Memory Arrays



Array Architecture

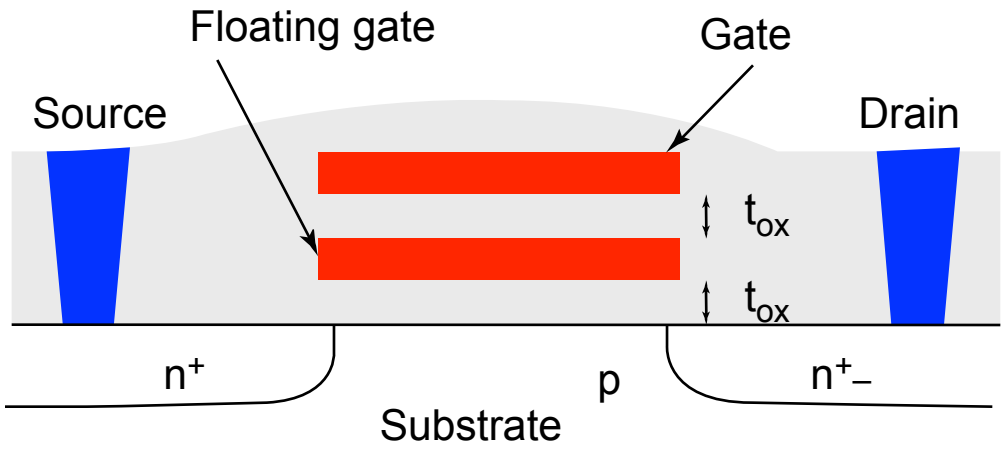
- 2^n *words* of 2^m *bits* each
- If n >> m, fold by 2^k into fewer *rows* of more *columns*



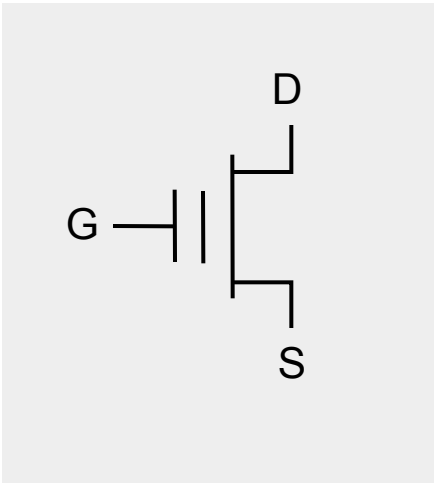
- Good regularity – easy to design
- Very high density if good cells are used

Non-Volatile Memories

- Floating-gate transistor

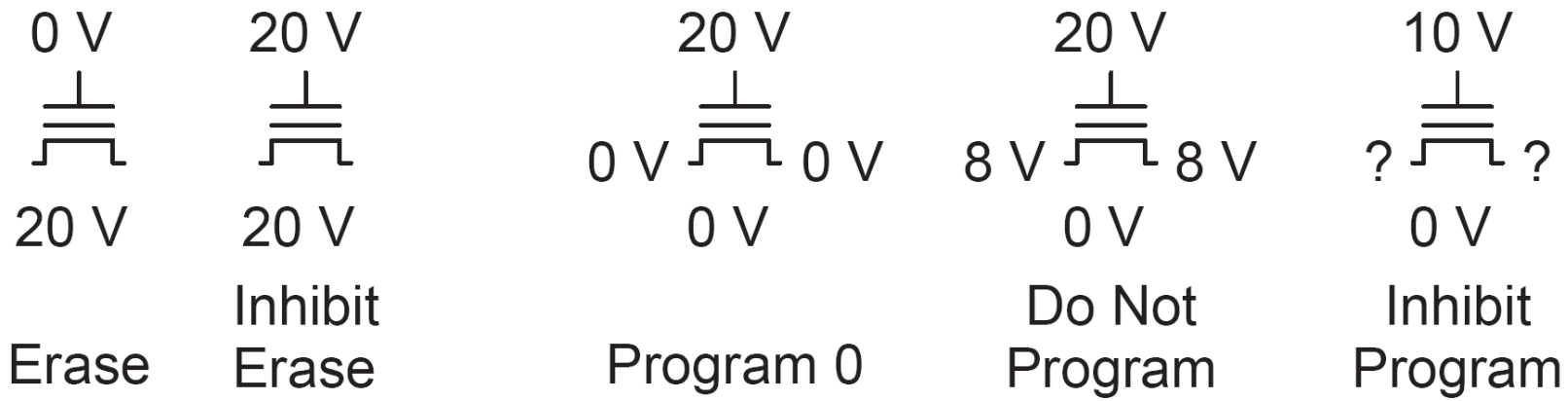


Device cross-section



Schematic symbol

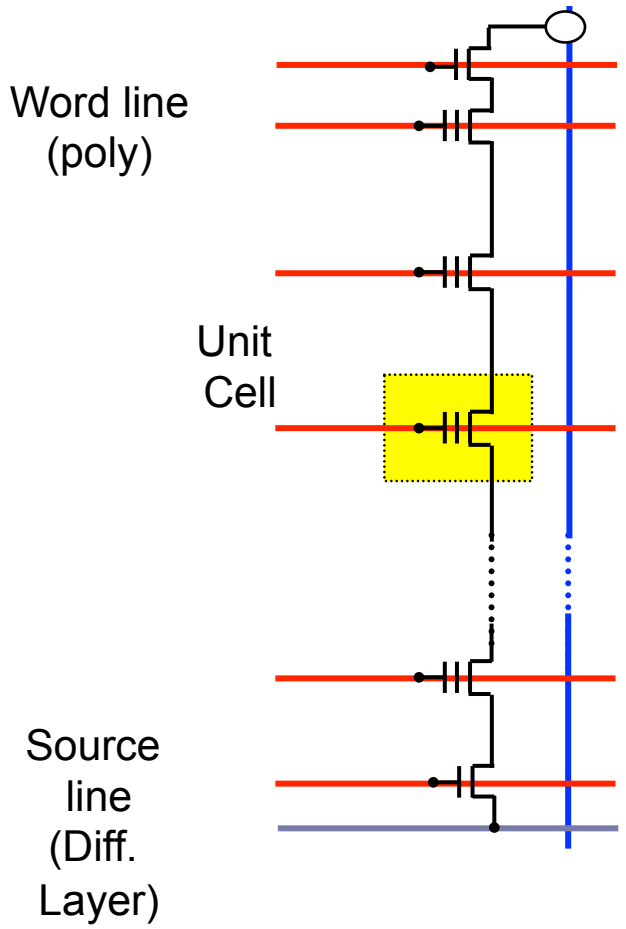
Floating-Gate Transistor Programming



FN Tunneling
Remove e-
Negative Vt
"1"

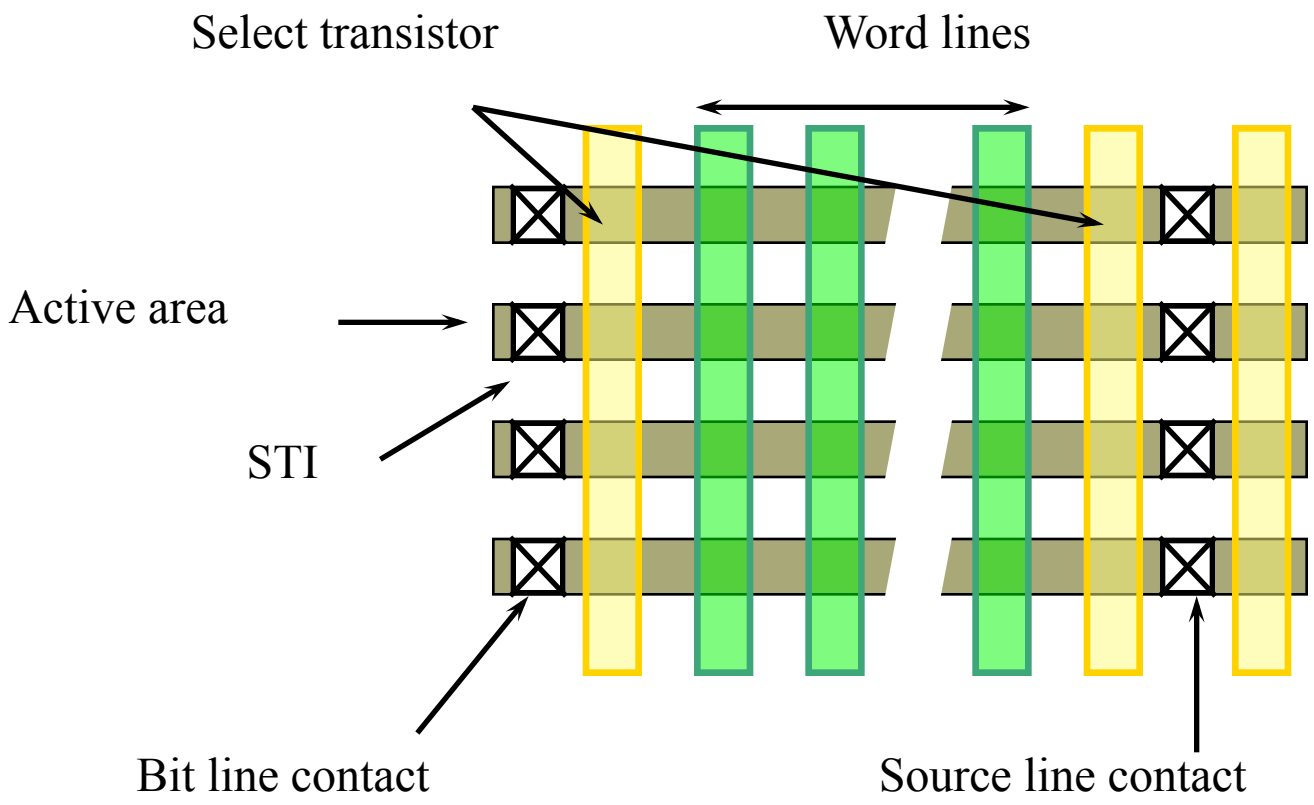
FN Tunneling
Add e-
Positive Vt
"0"

NAND Flash Memory



Courtesy Toshiba

NAND Flash Memory



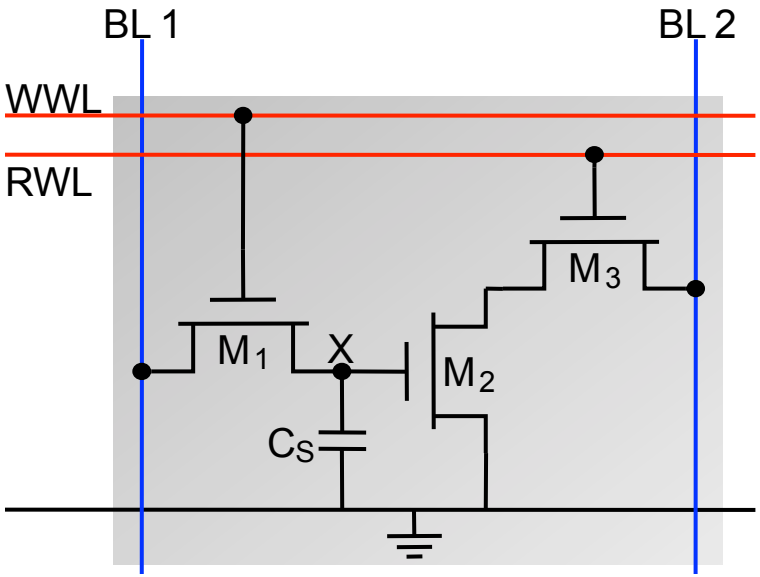
Courtesy Toshiba

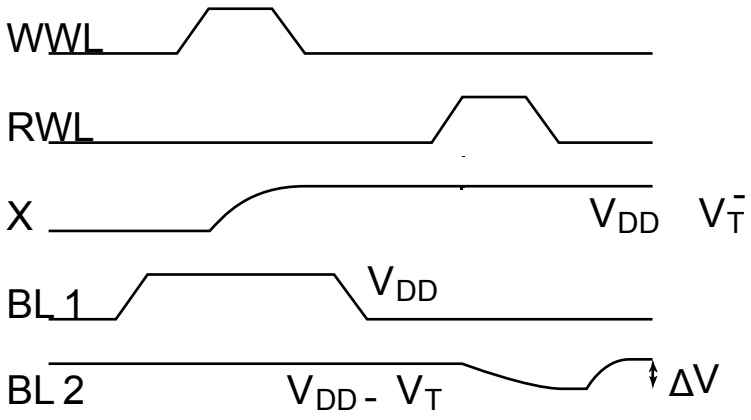
Read-Write Memories (RAM)

- Static (SRAM)
  - Data stored as long as supply is applied
  - Large (6 transistors/cell)
  - Fast
  - Differential
- Dynamic (DRAM)
  - Periodic refresh required
  - Small (1-3 transistors/cell)
  - Slower
  - Single Ended

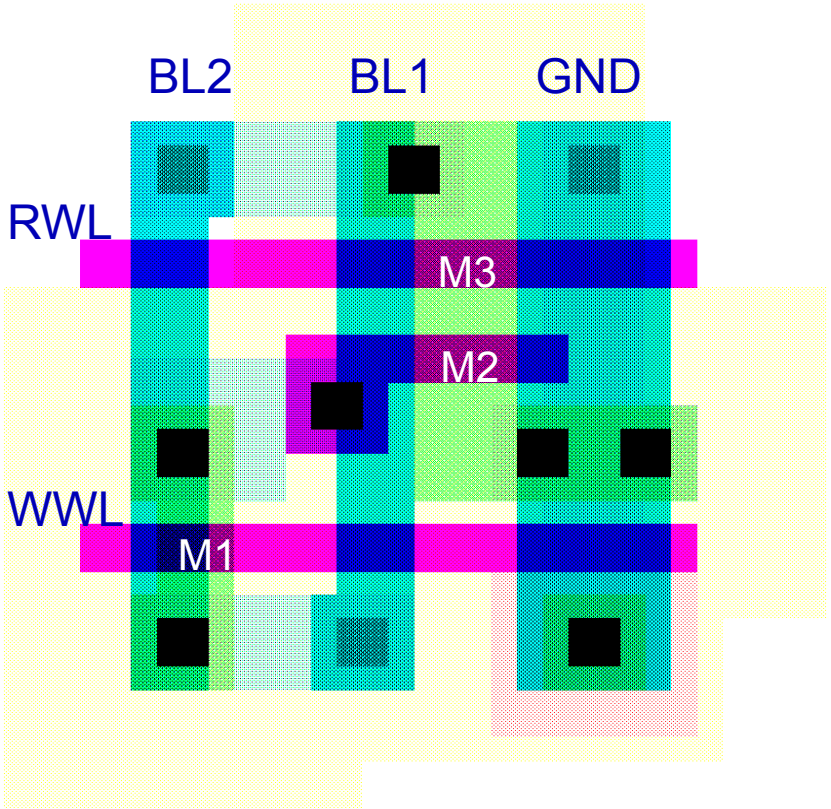
3-Transistor DRAM Cell

- No constraints on device ratios
- Reads are non-destructive
- Value stored at node X when writing a "1" = V_{wwl}-V_{tn}



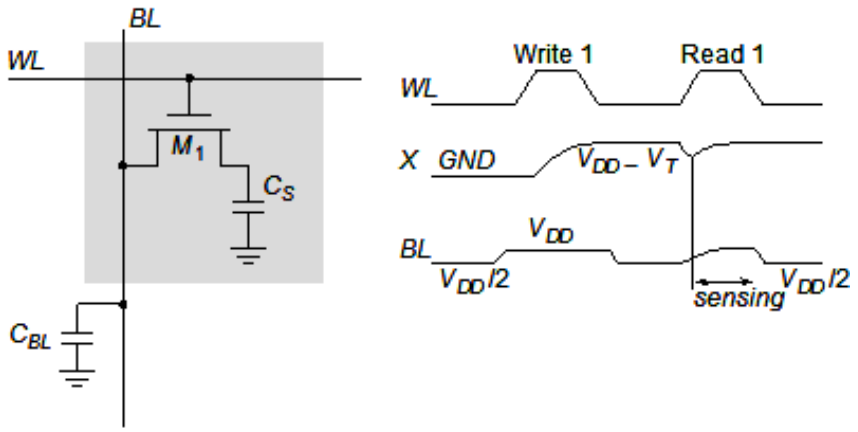


3T-DRAM — Layout



1-Transistor DRAM Cell

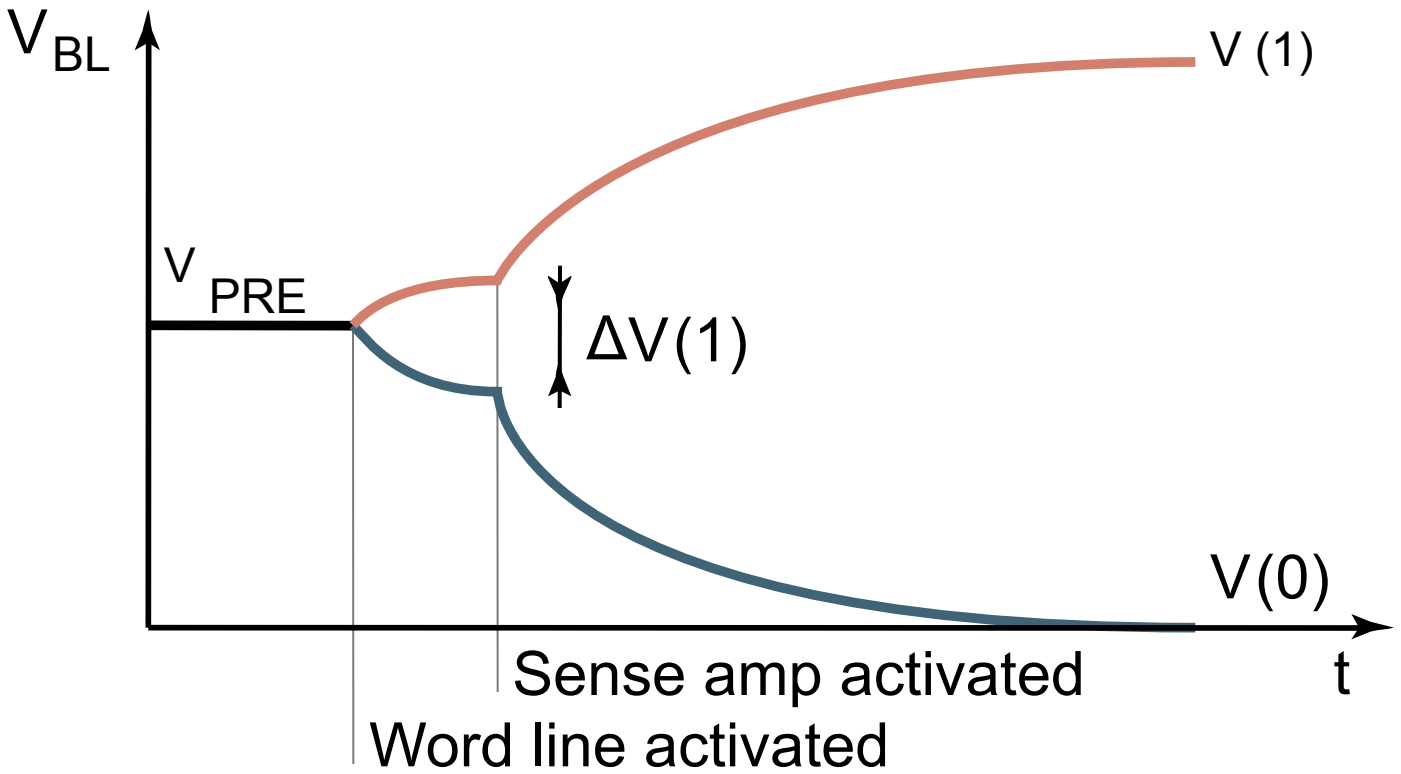
- Write: Cs is charged or discharged by asserting WL and BL
- Read: Charge redistribution takes place between bit line and storage capacitance
- Voltage swing is small; typically around 250 mV



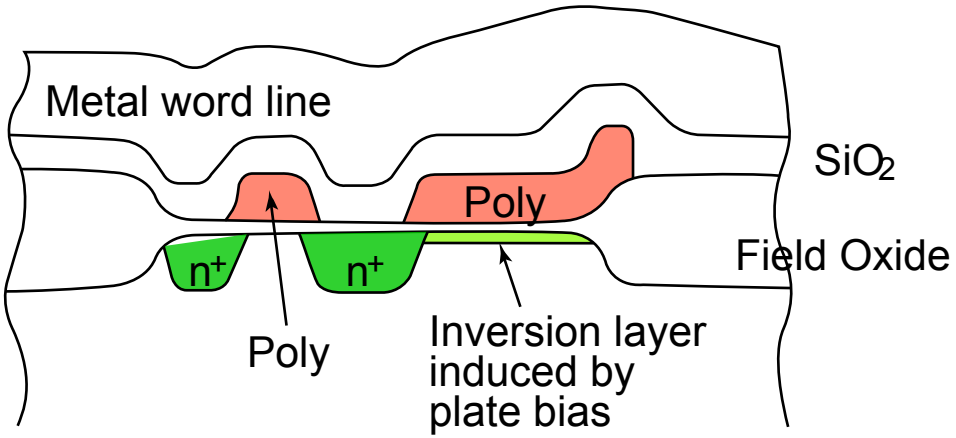
DRAM Cell Observations

- 1T DRAM requires a sense amplifier for each bit line, due to charge redistribution read-out.
- DRAM memory cells are single ended in contrast to SRAM cells.
- The read-out of the 1T DRAM cell is destructive; read and refresh operations are necessary for correct operation.
- Unlike 3T cell, 1T cell requires presence of an extra capacitance that must be explicitly included in the design.
- When writing a “1” into a DRAM cell, a threshold voltage is lost. This charge loss can be circumvented by bootstrapping the word lines to a higher value than V_{DD}

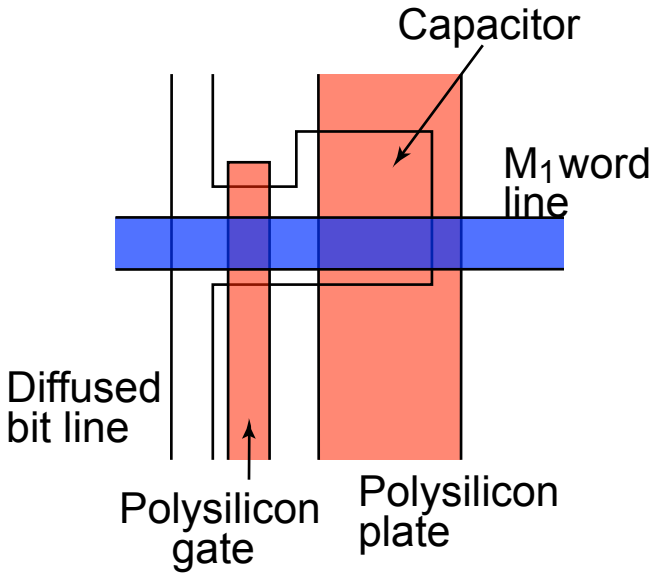
Sense Amp Operation



1-T DRAM Cell



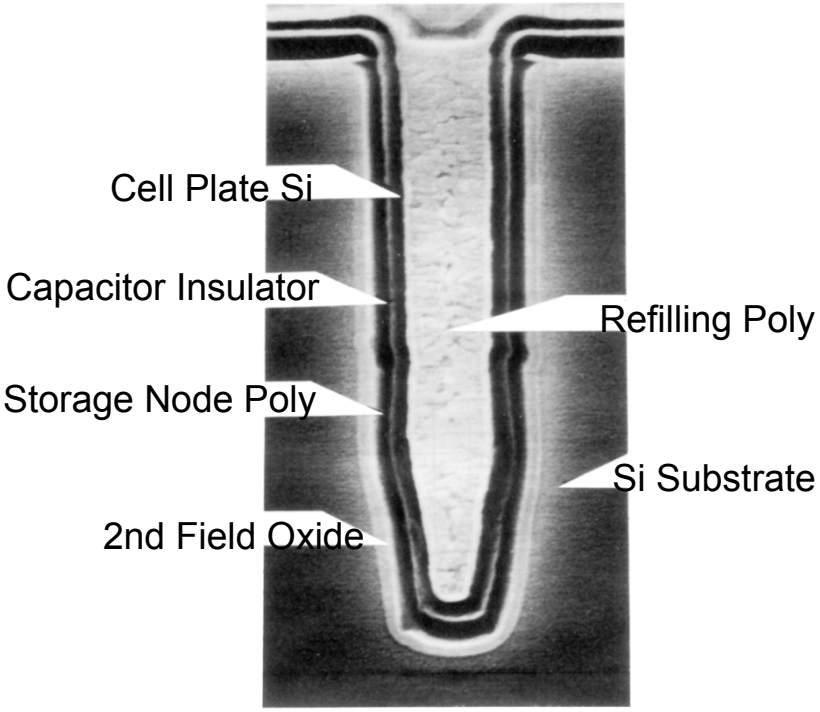
Cross-section



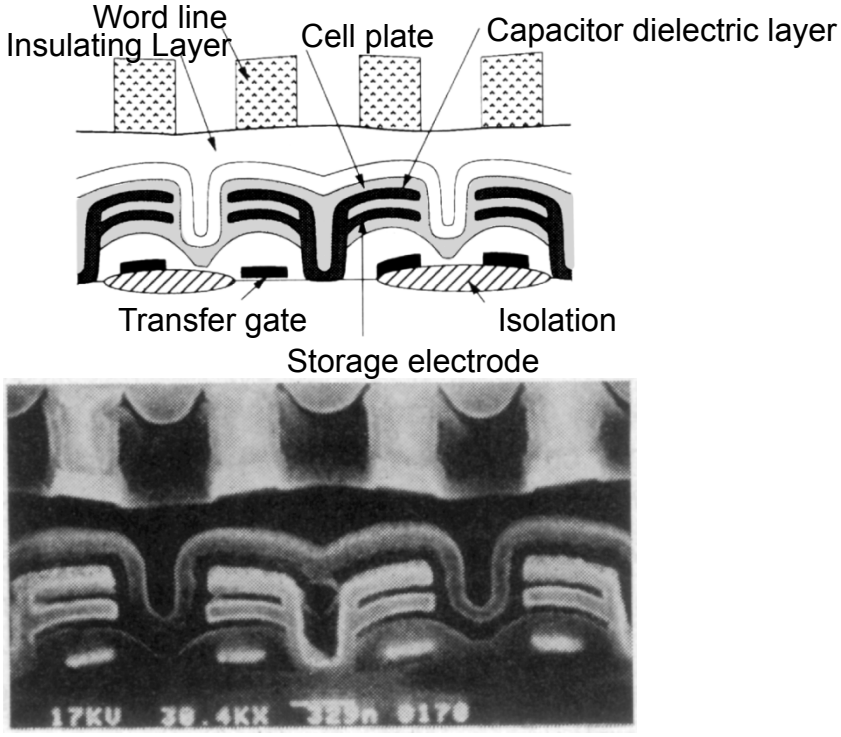
Layout

Uses Polysilicon-Diffusion Capacitance
Expensive in Area

Advanced 1T DRAM Cells

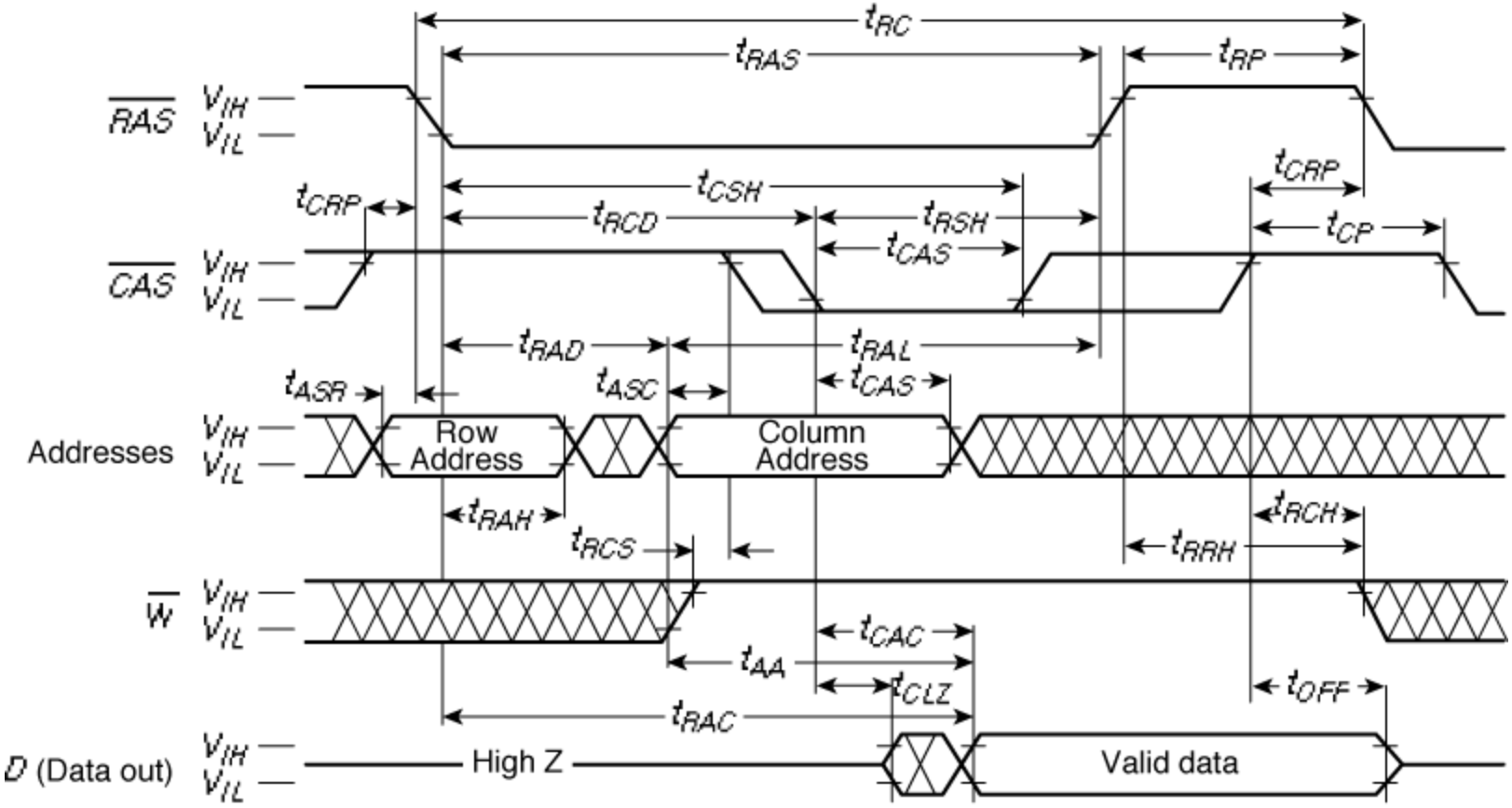


Trench Cell

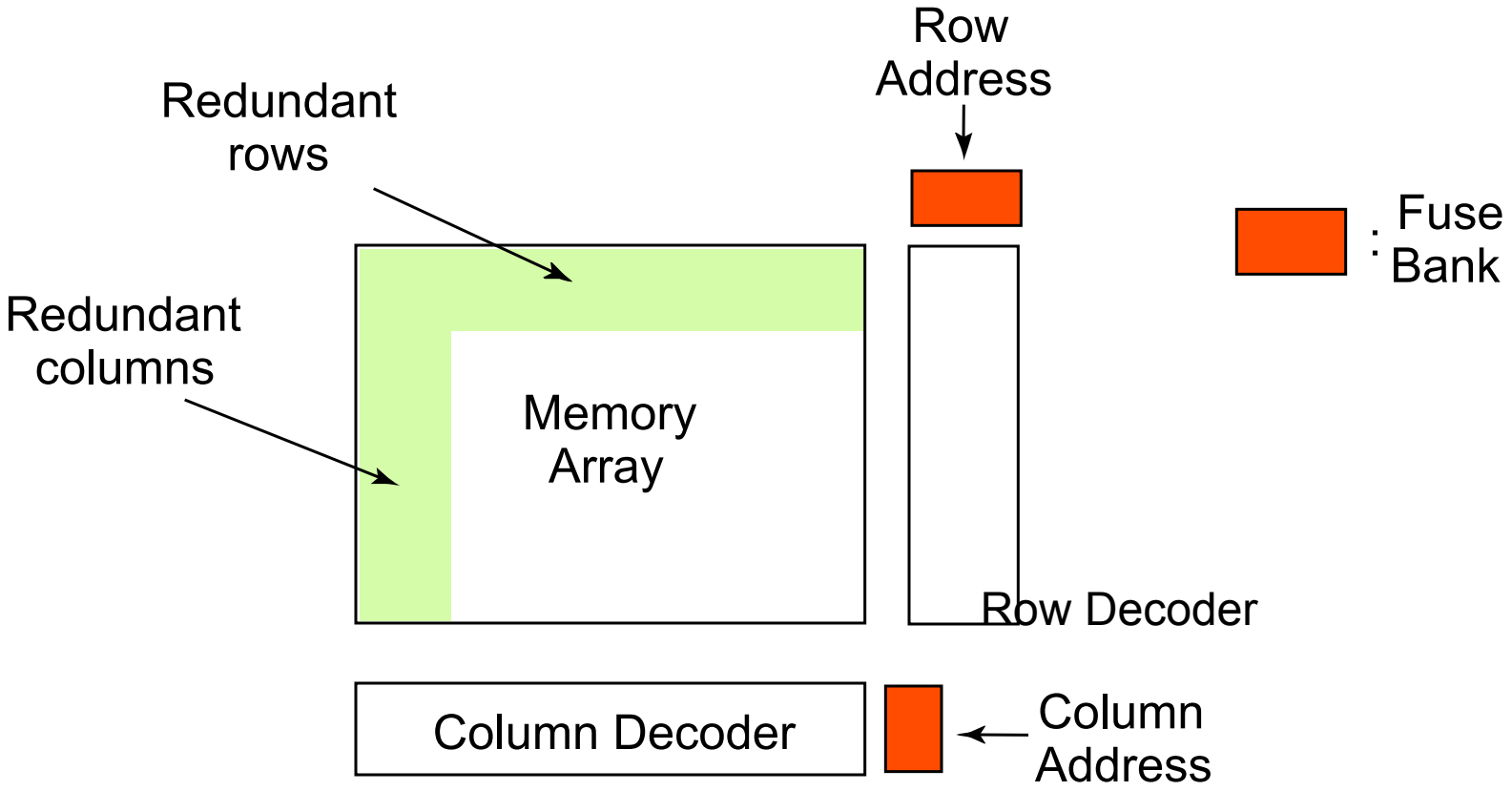


Stacked-capacitor Cell

DRAM Timing


t_{RC}
t_{RAS}
t_{RP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{CRP}
t_{CSH}
t_{RCD}
t_{RSH}
t_{CAS}
t_{CRP}
t_{CP}
$\overline{CAS}$
t_{RAD}
t_{RAL}
t_{ASR}
t_{ASC}
t_{CAS}
Addresses
Row Address
Column Address
t_{RAH}
t_{RCS}
t_{RCH}
t_{RRH}
$\overline{W}$
t_{CAC}
t_{AA}
t_{CLZ}
t_{OFF}
t_{RAC}
D (Data out)
High Z
Valid data

Redundancy


Row
Address
Redundant
rows
Fuse
Bank
Redundant
columns
Memory
Array
Row Decoder
Column Decoder
Column
Address