55:131 Introduction to VLSI Design

Stick Diagrams

Gate Layout

Layout can be very time consuming

- Design gates to fit together nicely
- Build a library of standard cells
- Standard cell design methodology
 - V_{DD} and GND should abut (standard height)
 - Adjacent gates should satisfy design rules
 - nMOS at bottom and pMOS at top
 - All gates include well and substrate contacts

Example: Inverter



Example: NAND3

- Horizontal N-diffusion and p-diffusion strips
- Vertical polysilicon gates
- Metal1 V_{DD} rail at top
- Metal1 GND rail at bottom
- \square 32 λ by 40 λ



Stick Diagrams

Stick diagrams help plan layout quickly

- Need not be to scale
- Draw with color pencils or dry-erase markers



Wiring Tracks

A wiring track is the space required for a wire
4 λ width, 4 λ spacing from neighbor = 8 λ pitch
Transistors also consume one wiring track



Well spacing

\square Wells must surround transistors by 6 λ

- Implies 12 λ between opposite transistor flavors
- Leaves room for one wire track



Area Estimation

Estimate area by counting wiring tracks

• Multiply by 8 to express in λ



Example: O3AI

Sketch a stick diagram for O3AI and estimate area $Y = (A + B + C) \cdot D$

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Problem 1.12



Problem 1.16

□ F=(AB+AC+BC)' = (AB + C(A+B))'



(c) 6 tracks wide x 7 tracks high = $(48 \times 56) = 2688 \lambda^2$.