55:131
Introduction to VLSI Design

Final Exam Preparation
Topics

- Sequential Circuits
  - Flip-Flops
  - Latches
  - Setup and Hold Timing
  - Skew

- Adders
  - Propagate and Generate Signals
  - Carry-Ripple Adder
  - Carry-Skip Adder
  - Carry-Lookahead Adder
  - Carry-Select Adder
Topics

- Datapath Units
  - Comparators
  - Shifters
  - Multipliers

- Memories
  - Arrays
  - Decoders
  - Column Circuitry
  - SRAM
  - DRAM
  - Flash
Topics, cont’d

- Design For Test
  - Fault Models
  - Observability and Controllability
  - Scan
  - BIST
  - Boundary Scan

- Chip-Level Issues
  - Packaging
  - Power Distribution
  - Clock Distribution
Topics, cont’d

- IO
  - Basic I/O Pads
  - I/O Channels
  - Transmission Lines
  - Noise and Interference
  - High-Speed I/O
  - Transmitters
  - Receivers
  - Clock Recovery
  - Source-Synchronous
  - Mesochronous
Other Notes

- If at all possible, make your design synchronous
  - One clock signal, delivered to each flop, without gating
    - State changes occur synchronously with clock
  - One reset signal, delivered to each flop, without gating
    - Puts circuit into a pre-defined (default) state
- Benefits of Synchronous design
  - Avoids hazards
  - Better noise immunity
  - Easier to design and debug
  - Better tool support
  - Many others!
- KISS Principle: Keep it Strictly Synchronous!
Other Notes

- Device verification generally costs as much or more than design
  - Plan it out and do it right

- Setup and hold times of flip-flops and latches must be met for reliable circuit operation
  - Write constraints
  - Do Static Timing Analysis
  - Pay attention to asynchronous inputs and signals that cross clock domains

- CMOS logic slows down with increasing temperature and decreasing supply voltage
  - Use the heat gun and freeze mist in the lab
These 3 nMOS transistors are in series. Current can flow from GND to Y when all three inputs are high (i.e. A=B=C=1).

These 3 pMOS transistors are in parallel. When any one of the inputs are low, the transistor(s) connect(s) adjacent contacts. This connects Y to Vdd through the one(s) that is (are) on.
Bad Synchronizer Designs

- Data must remain consistent