Topics

- CMOS gates
  - Inverter, NAND, NOR, compound
  - Pull-down, pull-up networks
  - Pass transistors, transmission gates, tri-states
  - Muxes, latches, flip-flops
- Stick Diagrams
  - Bring colored pencils if that would help you
- Tracks, spacing, area estimation
Topics, cont’d

- Fabrication
  - Masks
  - SiO$_2$
  - Polysilicon
  - Diffusion
  - Contacts
  - Wells
  - Metallization
  - Design Rules
  - Yield, Defects
Topics, cont’d

- MOSFET
  - MOS Capacitor
  - Accumulation, Depletion, Inversion
  - Modes of operation: Cutoff, Linear, Saturation
  - Shockley Models
  - Gate and diffusion capacitance
  - I-V characteristics
Topics, cont’d

- Nonideal Transistor Behavior
  - High Field Effects
  - Channel Length Modulation
  - Threshold Voltage Effects
  - Leakage
- Process and Environmental Variations
Topics, cont’d

- DC and Transient Response
  - Pass Transistors
  - DC Response
  - Logic Levels and Noise Margins
  - Transient Response
  - RC Delay Models
  - Delay Estimation
Topics, cont’d

- Logical Effort
  - Delay in a Logic Gate
  - Multistage Logic Networks
  - Choosing the Best Number of Stages
Topics, cont’d

- Interconnect Wires
  - Interconnect Modeling
    - Wire Resistance
    - Wire Capacitance
  - Wire RC Delay
  - Crosstalk
  - Wire Engineering
  - Repeaters
Topics, cont’d

- Power
  - Power and Energy
  - Dynamic Power
  - Static Power
Topics, cont’d

- Combinational Circuit Design
  - Bubble Pushing
  - Compound Gates
  - Input Ordering
  - Asymmetric Gates
  - Skewed Gates
  - Best P/N ratio
Topics, cont’d

- Circuit Families
  - Pseudo-nMOS logic
  - Dynamic logic
  - Pass transistor logic