Case Study of a Multi-core, Multi-threaded Processor—The Sun T1 (“Niagara”)

Reference


T1 (“Niagara”)

- Target: Commercial server applications
  - High thread level parallelism (TLP)
    - Large numbers of parallel client requests
  - Low instruction level parallelism (ILP)
    - High cache miss rates
    - Many unpredictable branches
    - Frequent load-load dependencies
- Power, cooling, and space are major concerns for data centers
- Approach: Multicore, Fine-grain multithreading, Simple pipeline, Small L1 caches, Shared L2

T1 Architecture

- Also ships with 6 or 4 processors

![T1 Architecture Diagram]
T1 pipeline

- Single issue, in-order, 6-deep pipeline: F, S, D, E, M, W
- 3 clock delays for loads & branches.
- Shared units:
  - L1 $, L2 $ – L1 $, L2 $, TLB, X units, pipe registers
- Hazards:
  - Data
  - Structural

Integer Register File

- One register file / thread
- SPARC window: in, out, local registers
- Highly integrated cell structure to support 4 threads:
  - 8 windows of 32 locations / thread
  - 3 read ports + 2 write ports
  - Read/write: single cycle latency
- 1 Active Window Cell (copy of the architectural set window)

Thread Scheduling

- Thread selection based on:
  - Previous long latency instruction in pipe
  - Instruction type
  - LRU status
- Select & Fetch coupled

T1 Fine-Grained Multithreading

- Each core supports four threads and has its own level one caches (16KB for instructions and 8 KB for data)
- Switching to a new thread on each clock cycle
- Idle threads are bypassed in the scheduling
  - Waiting due to a pipeline delay or cache miss
  - Processor is idle only when all 4 threads are idle or stalled
- Both loads and branches incur a 3 cycle delay that can only be hidden by other threads
- A single set of floating point functional units is shared by all 8 cores
  - Floating point performance was not a focus for T1
Memory, Clock, Power

- 16 KB 4 way set assoc. I$ core
- 8 KB 4 way set assoc. D$ core
- 3MB 12 way set assoc. L2 $ shared
  - 4 x 750KB independent banks
  - crossbar switch to connect
  - 2 cycle throughput, 8 cycle latency
  - Direct link to DRAM & Jbus
  - Manages cache coherence for the 8 cores
  - CAM based directory
- Coherency is enforced among the L1 caches by a directory associated with each L2 cache block
- Used to track which L1 caches have copies of an L2 block
- By associating each L2 with a particular memory bank and enforcing the subset property, T1 can place the directory at L2 rather than at the memory, which reduces the directory overhead
- L1 data cache is write-through, only invalidation messages are required; the data can always be retrieved from the L2 cache
- 1.2 GHz at ~72W typical, 79W peak power consumption

Write through
- allocate LD
- no-allocate ST

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Miss Rates: L2 Cache Size, Block Size

CPI Breakdown of Performance

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Per Thread CPI</th>
<th>Per core CPI</th>
<th>Effective CPI for 8 cores</th>
<th>Effective IPC for 8 cores</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPC-C</td>
<td>7.20</td>
<td>1.80</td>
<td>0.23</td>
<td>4.4</td>
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<tr>
<td>SPECJBB</td>
<td>5.60</td>
<td>1.40</td>
<td>0.18</td>
<td>5.7</td>
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<tr>
<td>SPECWeb99</td>
<td>6.60</td>
<td>1.65</td>
<td>0.21</td>
<td>4.8</td>
</tr>
</tbody>
</table>
Not Ready Breakdown

- TPC-C - store buffer full is largest contributor
- SPEC-JBB - atomic instructions are largest contributor
- SPECWeb99 - both factors contribute

Performance: Benchmarks + Sun Marketing

<table>
<thead>
<tr>
<th>Benchmark/Architecture</th>
<th>Sun Fire T2000</th>
<th>IBM p5-550 with 2 dual-core Power5 chips</th>
<th>Dell PowerEdge</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECjbb2005 (Java server software)</td>
<td>63,378</td>
<td>61,789</td>
<td>24,208 (SC1425 with dual single-core Xeon)</td>
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<tr>
<td>SPECweb2005 (Web server performance)</td>
<td>14,661</td>
<td>7,881</td>
<td>4,850 (2850 with two dual-core Xeon processors)</td>
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<tr>
<td>NotesBench (Lotus Notes performance)</td>
<td>16,661</td>
<td>14,740</td>
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</table>

<table>
<thead>
<tr>
<th>Processor</th>
<th>SUN T1</th>
<th>Opteron</th>
<th>Pentium D</th>
<th>IBM Power 5</th>
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</thead>
<tbody>
<tr>
<td>Cores</td>
<td>8</td>
<td>2</td>
<td>2</td>
<td>2</td>
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<tr>
<td>Instruction issues</td>
<td>1</td>
<td>3</td>
<td>3</td>
<td>4</td>
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<tr>
<td>Peak instr. issues</td>
<td>8</td>
<td>6</td>
<td>6</td>
<td>8</td>
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<tr>
<td>Multithreading</td>
<td>Fine-grained</td>
<td>No</td>
<td>SMT</td>
<td>SMT</td>
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<tr>
<td>L1 I/D in KB per core</td>
<td>16/8</td>
<td>64/64</td>
<td>12K</td>
<td>64/32</td>
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<tr>
<td>L2 per core/shared</td>
<td>3 MB</td>
<td>1MB/16</td>
<td>1MB/16</td>
<td>1.9 MB shared</td>
</tr>
<tr>
<td>Clock rate (GHz)</td>
<td>1.2</td>
<td>2.4</td>
<td>3.2</td>
<td>1.9</td>
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<tr>
<td>Transistor count (M)</td>
<td>300</td>
<td>233</td>
<td>230</td>
<td>276</td>
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<tr>
<td>Die size (mm²)</td>
<td>379</td>
<td>199</td>
<td>206</td>
<td>389</td>
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<tr>
<td>Power (W)</td>
<td>79</td>
<td>110</td>
<td>130</td>
<td>125</td>
</tr>
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</table>

Note the paradigm shift
Niagara 2

- Improve performance by increasing threads supported per chip from 32 to 64
  - 8 cores * 8 threads per core
- Floating-point unit for each core, not for each chip
- Hardware support for encryption standards EAS, 3DES, and elliptical-curve cryptography
- Niagara 2 will add a number of 8x PCI Express interfaces directly into the chip in addition to integrated 10Gigabit Ethernet XAU interfaces and Gigabit Ethernet ports.
- Integrated memory controllers will shift support from DDR2 to FB-DIMMs and double the maximum amount of system memory.

Sun Niagara 2 at a Glance

- 8 cores x 8 threads = 64 threads
- Dual single issue pipelines
- 1 FPU per core
- 4MB L2, 8-banks, 16-way S.A
- 4 x dual-channel FB-DIMM ports (60+ GB/s)
- > 2x Niagara 1 throughput and throughput/watt
- 1.4 x Niagara 1 int
- > 10x Niagara 1 FP
- Available H2 2007

Kevin Krewell
"Sun’s Niagara Begins CMT Flood - The Sun UltraSPARC T1 Processor Released"
Microprocessor Report, January 3, 2006