Case Study: A Modern Superscalar Architecture—Intel Nehalem

55:132/22C:160
Spring, 2011

References

Nehalem Architecture—More detailed view

Loop Detection—Core 2 versus Nehalem

Nehalem O-O-O Execution Unit

Nehalem: Claimed Performance Gains due to SMT (Hyperthreading)
Nehalem Memory Hierarchy

Nehalem Cache Coherency Protocol

Comparison of MESI, MESIF, MEOSI
Nehalem Power Management

- Integrated proprietary microcontroller
- Shifts power to unneeded firmware
- Real-time awareness for temperature, current, power
- Flexibility enables sophisticated algorithms, tuned for current operating conditions

Nehalem Power-saving states

<table>
<thead>
<tr>
<th>Active state</th>
<th>C0</th>
<th>C1</th>
<th>C3</th>
<th>C6</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core clock</td>
<td>on</td>
<td>off</td>
<td>off</td>
<td>off</td>
</tr>
<tr>
<td>PLL</td>
<td>on</td>
<td>off</td>
<td>off</td>
<td>off</td>
</tr>
<tr>
<td>Core caches</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Shared cache</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Wakeup time</td>
<td>≈ 1s</td>
<td>≈ 1s</td>
<td>≈ 1s</td>
<td>≈ 0s</td>
</tr>
<tr>
<td>Core idle power*</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*N: rough approximation

Nehalem: Allocation of chip real-estate