Overview of Final Exam Topics

Final Exam Information

- Exam Time and Place:
  - Monday, May 9, noon-2:00 p.m.
  - 4030 SC
- Exam Details
  - Closed-book, closed notes—one 8.5" by 11" (one side) page of notes permitted
  - Exam is not comprehensive—will cover material since midterm
  - Format will be similar to midterm—perhaps slightly more conceptual
- Remember:
  - Better of midterm and final exam scores counts 35% toward final grade
  - Poorer of midterm and final scores counts 25%
Final Exam Coverage

• Lecture Notes:
  – Material beginning with Slide 60 of Sixth Lecture Note Set (VLIW)

• Text:
  – Appendix G (VLIW)
  – Chapter 3 (Limits to ILP, Thread-level Parallelism)
  – Appendix C (Memory Hierarchy)
  – Chapter 5, except section 5.4 (Memory Hierarchy)
  – Chapter 4 (Multiprocessors)

Final Exam Topical Coverage

• VLIW
• Thread-level parallelism
  – Fine-grained
  – Coarse-grained
  – SMT
• Memory Hierarchy
  – Underlying principles
    • Locality
    • More reads than writes
  – Cache Memory
    • Basic notions: miss rates, miss penalties, etc
    • Cache organizations: direct-mapped, set-associative, fully associative
    • Replacement policies
    • Write policies
    • Miss rates: The three Cs
    • Multilevel caches
    • Calculating cache performance
    • Cache Optimizations
Final Exam Topical Coverage (continued)

• Main Memory Organization
  – Interleaving
• Virtual Memory
  – Virtual versus Physical Address Space
  – Paged virtual memory organization
  – Multi-level page tables
  – TLB
• Multiprocessors
  – Flynn’s taxonomy
  – Multiprocessor Organization: Centralized versus distrib. Memory, SMT versus NUMA
  – Cache coherence
    • Snoopy cache coherence: MSI, MESI, MOSI
    • Directory-based coherence protocols (just the general concept)
    • The fourth C: Coherency misses

Final Exam Topical Coverage (continued)

• Case Studies
  – PPC 620
  – Intel P6
  – Intel Nehalem
  – Sun (Oracle) T1-T3